Printed Circuit Board

Design, Development and Fabrication Process

This presentation is courtesy of

Tom Lee
Printed Circuit Board Design Engineer
From FMUSER

Introduction

PCB 101

This presentation outlines the printed circuit board design process, and the details required to capture design intent.

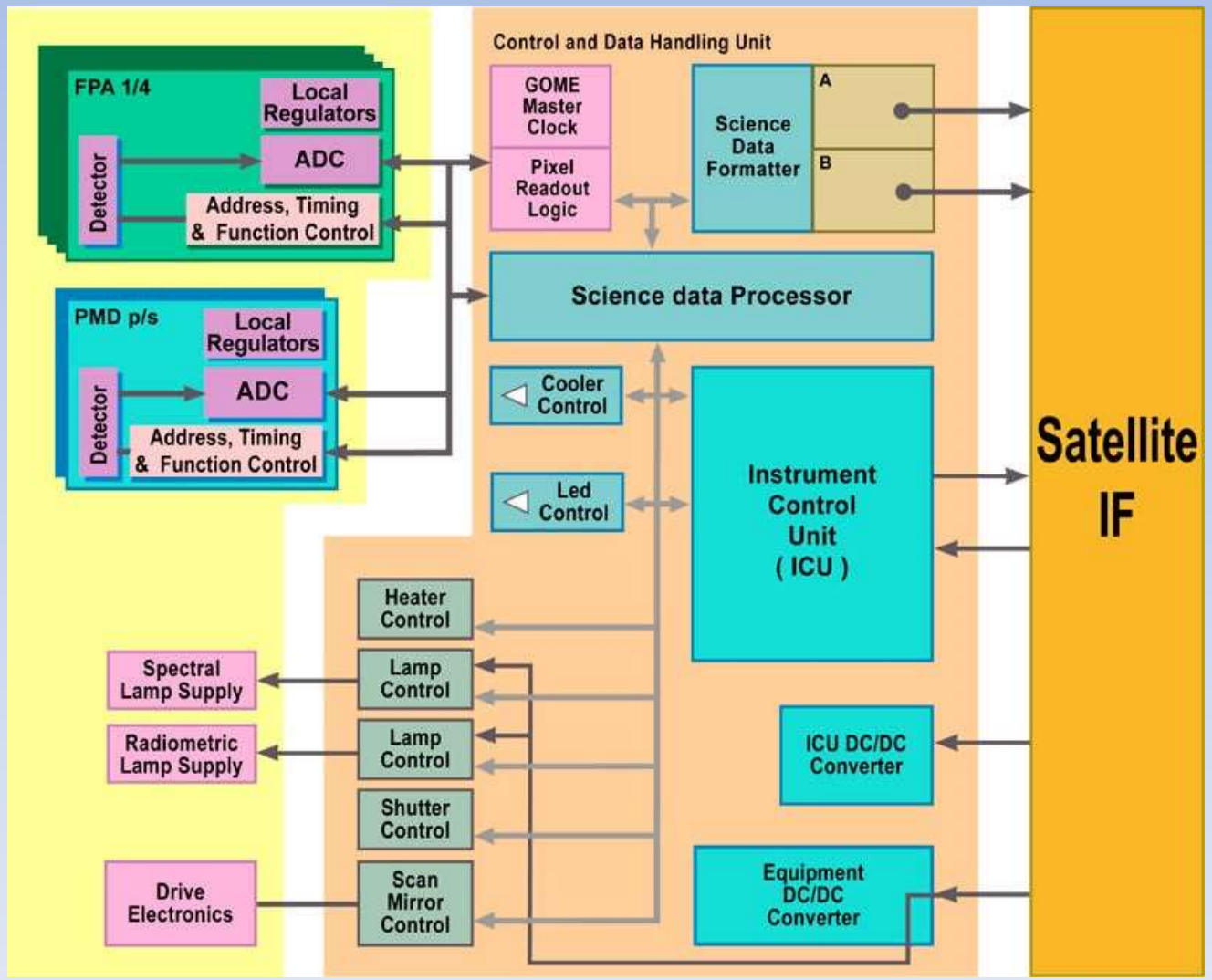
These guidelines were created to ensure an error-free robust design that will meet or exceed cost expectations, satisfy fabrication, assembly and test criteria, and conform to form, fit and function requirements.

Design Process Overview

- Concept
- Electrical Architect
- Electrical Component Selection
- Schematic
- Bill of Materials
- PCB Library Component Development
- Netlist
- PCB Netlist Verification
- Mechanical Inputs
- Design Requirements
- PCB Design
- PCB Design Verification
- Gerber File Generation
- PCB DFT / DFM
- Design Review (Preliminary)
- Incorporate Design Review and DFT/ DFM Feedback
- Overlay Output
- Gerber Analysis and Plotfile Verification
- Panelize PCB
- Finalize Gerber Fabrication Package
- PCB Fabrication

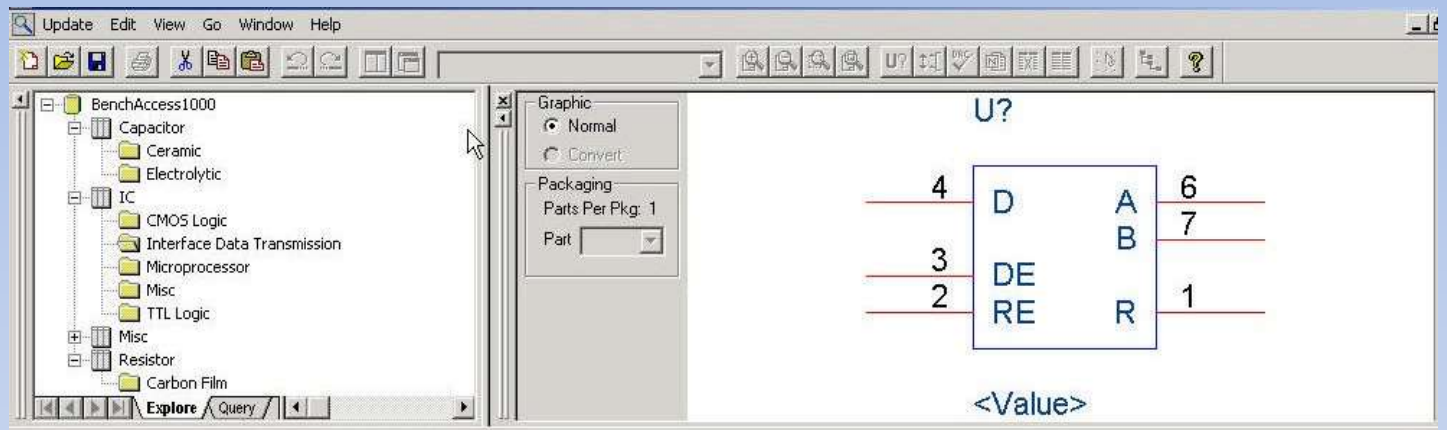
Electrical Architect

A fundamental design strategy is developed and an electrical hierarchy is established.



Electrical Component Selection

Components that will be used in the electrical schematic are selected and designed.

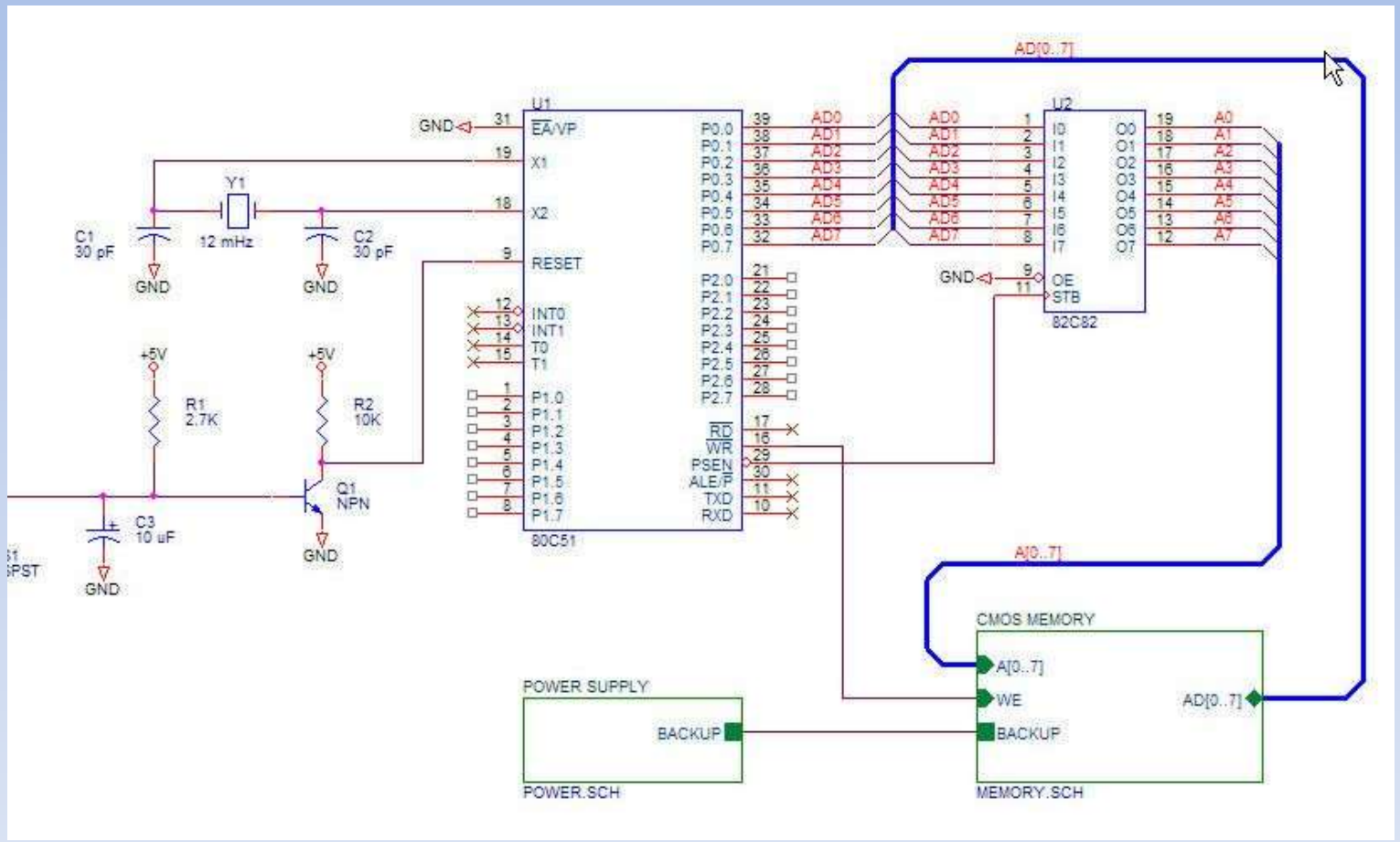


	Property	Database Contents	Visible
1	Implementation		☑
2	PCB Footprint	DIP.100/8/W.300/L.400	☐
3	Value	75176	☑
4	Part Number	20-00176BTN	☑
5	Schematic Part	75176	☑
6	Part Type	Interface Data Transmis	☑
7	Description	IC, MULITPOINT RS485 T	☑
8	Allegro PCB Footprint	dip8_3	☑
9	Manufacturer Part Nu	DS75176BTN	☑
10	Manufacturer	National Semiconductor	☑
11	Distributor Part Numbe	DS75176BTN-ND	☑

	Table	Part Number	Part Type	Value	Description	Schematic Part	PCB Footprint	Allegro PCB Footprint	Implementation	Manufacturer Part Number	Manufacturer	Distributor Part Number	Distributor	Pri
1	IC	20-00176	Interface Dat	75176	IC, RS485/RS	75176	DIP.100/8/W.3	dip8_3		DS75176BN	National Semi	DS75176BN-	Digi-Key	1.05
2	IC	20-00176BTN	Interface Dat	75176	IC, MULITPOIN	75176	DIP.100/8/W.3	dip8_3		DS75176BTN	National Semi	DS75176BTN	Digi-Key	1.58
3	IC	20-00176BM	Interface Dat	75176	IC, MULTI RS4	75176	SOG.050/8/W	soic8		DS75176BM	National Semi	DS75176BM-	Digi-Key	1.05
4	IC	20-00176BTM	Interface Dat	75176	IC, MULITPOIN	75176	SOG.050/8/W	soic8		DS75176BTM	National Semi	DS75176BTM	Digi-Key	3.5

Schematic

The electrical components are placed in the schematic and net connections established.



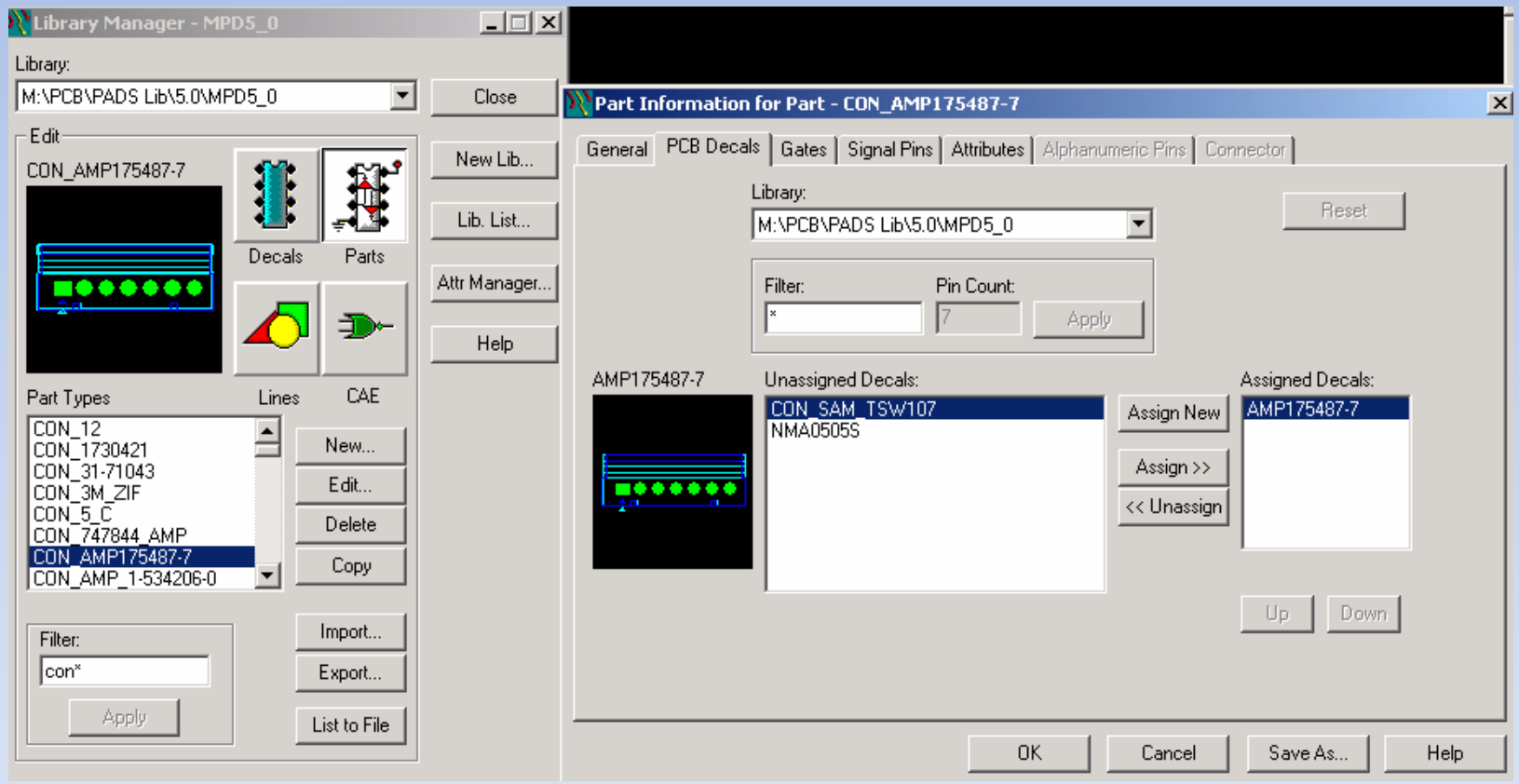
Bill of Materials

The Bill of Materials is derived from the components that exist in the schematic.

Item	Quantity	eferenc	Part	Value	Decal	MFG Part Number	Datasheet
1	1	C1	1000PF	+/-1% 50V	1206	GRM3195C1H102FA01B	..\..\MurataCerCap.pdf
2	2	C2	.01UFD	+/-5% 50V	1206	GRM3195C1H103JA01J	..\..\MurataCerCap.pdf
		C14	.01UFD	+/-5% 50V	1206	GRM3195C1H103JA01J	..\..\MurataCerCap.pdf
3	1	C3	4.7UFD	+/-10% 50V	1812	GRM43ER71E475KA01L	..\..\GRM43ER71E475KA01L.pdf
4	5	C4	33ufd 25V	+/-10% 25V	C-CASE	B45196E5336K30	..\..\B45196E5336K30.pdf
		C5	33ufd 25V	+/-10% 25V	C-CASE	B45196E5336K30	..\..\B45196E5336K30.pdf
		C6	33ufd 25V	+/-10% 25V	C-CASE	B45196E5336K30	..\..\B45196E5336K30.pdf
		C8	33ufd 25V	+/-10% 25V	C-CASE	B45196E5336K30	..\..\B45196E5336K30.pdf
		C16	33ufd 25V	+/-10% 25V	C-CASE	B45196E5336K30	..\..\B45196E5336K30.pdf
5	5	C7	.1UFD	+/-10% 50V	0603	GRM188R71H104KA93J	..\..\MurataCerCap.pdf
		C11	.1UFD	+/-5% 50V	1206	GRM319R71H104JA01L	..\..\MurataCerCap.pdf
		C12	.1UFD	+/-5% 50V	1206	GRM319R71H104JA01L	..\..\MurataCerCap.pdf
		C13	.1UFD	+/-5% 50V	1206	GRM319R71H104JA01L	..\..\MurataCerCap.pdf
		C15	.1UFD	+/-5% 50V	1206	GRM319R71H104JA01L	..\..\MurataCerCap.pdf
6	1	C9	1UFD	+/-10% 50V	1206	GRM31MR71H105KA88L	..\..\MurataCerCap.pdf
7	1	C10	.001UFD	+/-1% 50V	1206	GRM3195C1H102FA01B	..\..\MurataCerCap.pdf
8	1	D1	MBRS120T3	-	403A	MBRS120T3	..\..\MBRS120T3-D.pdf
9	2	D2	MRA4003T3	-	403D	MRA4003T3	..\MRA4003T3.pdf
		D3	MRA4003T3	-	403D	MRA4003T3	..\MRA4003T3.pdf
10	6	D4	IN4148	-	MELF3	LS4148	..\..\ln4148.pdf
		D5	IN4148	-	MELF3	LS4148	..\..\ln4148.pdf
		D6	IN4148	-	MELF3	LS4148	..\..\ln4148.pdf
		D7	IN4148	-	MELF3	LS4148	..\..\ln4148.pdf
		D8	IN4148	-	MELF3	LS4148	..\..\ln4148.pdf
		D9	IN4148	-	MELF3	LS4148	..\..\ln4148.pdf
11	1	D10	SMCJ16A	-	DO-214AB	SMCJ16A	..\..\smcjxxx.pdf
12	1	F1	FUSE	-	2010	LBC-LBZ2010-B000	..\..\LBZ.pdf

PCB Component Development

The components that reside on the pcb are designed from the Bill of Materials.
These pcb library parts are captured in the netlist, and consist of a decal and a part name.



Netlist

The netlist is typically an ASCII format generated from the schematic. It contains all components (*part*) and connections (*net*) required for the pcb design.

78727-0122r06.asc - Notepad

File Edit Format Help

```
!PADS-POWERPCB-V3.5-MILS!

*CLUSTER* ITEM


*PART*
Q5 2N7002W
Q9 2N7002W
Q12 2N7002W
Q13 2N7002W
U27 74AHCT1G32DCK
U36 74AHCT1G32DCK
U33 74VHC138MTC
U40 74VHC138MTC
U16 AD5231
U29 AD5231
U35 AD5231
U43 AD5231
U37 AD7888BRU
U38 AD7888BRU
U59 AD7888BRU
U60 AD7888BRU
U5 AD8602ARM
U7 AD8602ARM
U18 AD8602ARM
U47 AD8602ARM
U17 AD8604ARU
U19 AD8604ARU
U20 AD8604ARU
U23 AD8604ARU
U24 AD8604ARU
U25 AD8604ARU
U55 ADN8830ACP
U56 ADN8830ACP
Q10 BSS138@SOT23
Q11 BSS138@SOT23
C1 CAP0402
C2 CAP0402
C3 CAP0402
C4 CAP0402
C5 CAP0402
C6 CAP0402
C7 CAP0402
```

78727-0122r06.asc - Notepad

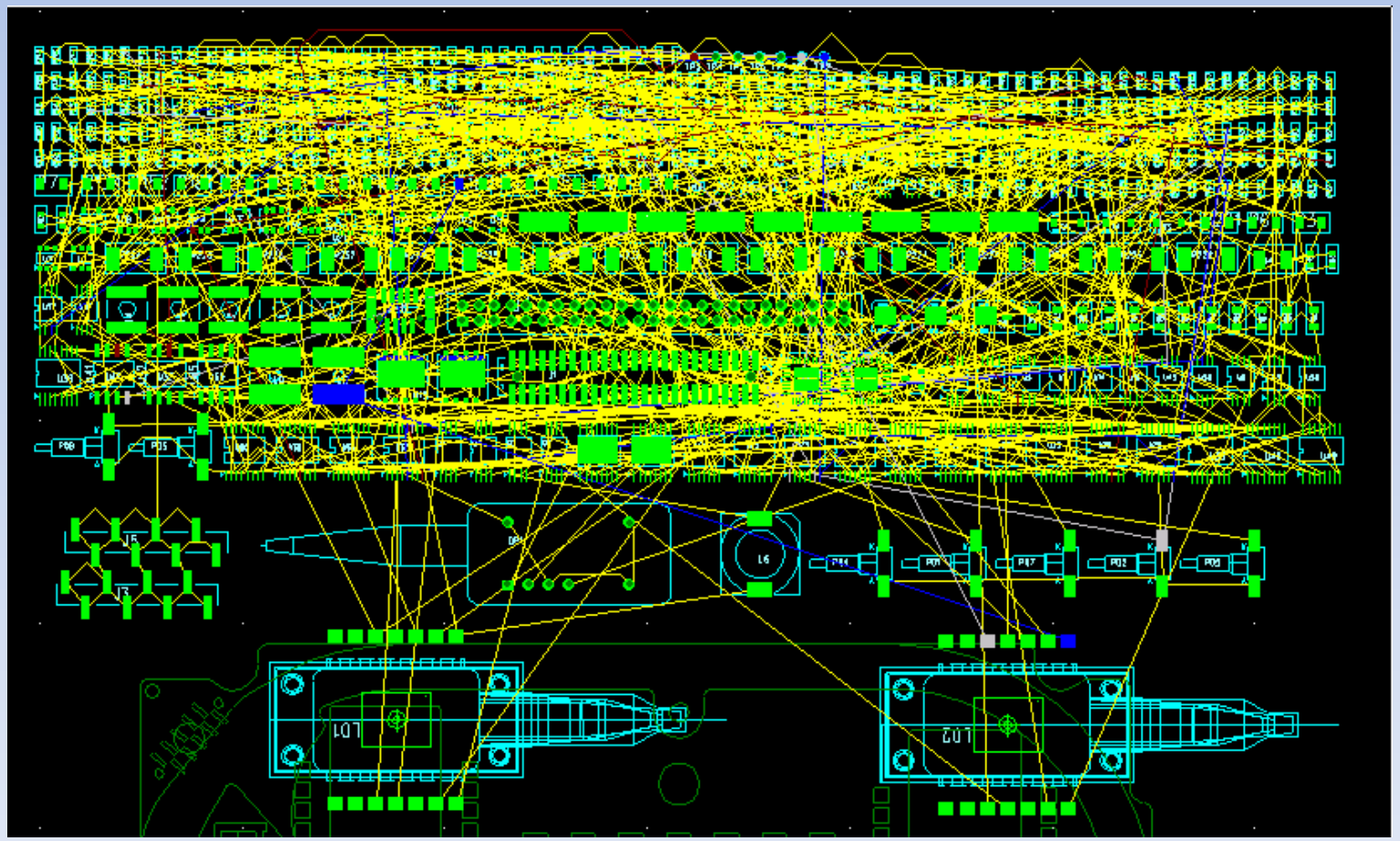
File Edit Format Help

```
OP1 VOA_JDS_MEMS_TH@VOA_JDS_MEMS_TH

*NET*
Q5.1 R59.2 U27.4
*SIGNAL* $4N925
Q9.1 R294.2 U36.4
*SIGNAL* $4N940
Q6.1 Q6.2 Q6.5 Q6.6 R26.2 R194.2
*SIGNAL* $3N1197
C153.1 R195.1 U14.7
*SIGNAL* $3N1206
C153.2 R194.1 R239.2 U14.6
*SIGNAL* $3N1331
R2.1 R28.2 U14.5
*SIGNAL* $3N1349
C53.2 R27.1 R172.2 U11.3
*SIGNAL* $3N1358
D6.A L8.2 U11.1
*SIGNAL* $3N1381
Q6.3 R195.2
*SIGNAL* $3N1420
J4.39 R276.2 R278.2
*SIGNAL* $3N1422
J4.40 R277.1 R279.1
*SIGNAL* $3N1445
Q8.3 Q8.6 R280.1
*SIGNAL* $3N1450
Q8.2 Q8.5 R281.2 R311.1
*SIGNAL* $3N1456
TP9.1 TP10.1 U7.1 U7.2
*SIGNAL* $3N1463
R281.1 U22.5
*SIGNAL* $3N1472
C36.1 R199.2 U22.1
*SIGNAL* $3N1474
C142.1 R282.2 U22.3
*SIGNAL* $3N1477
C151.2 R30.1 R282.1 R283.2
*SIGNAL* $3N1520
Q7.A1 R280.2
*SIGNAL* $4N299
C58.1 R31.2 U3.3
*SIGNAL* $4N314
```

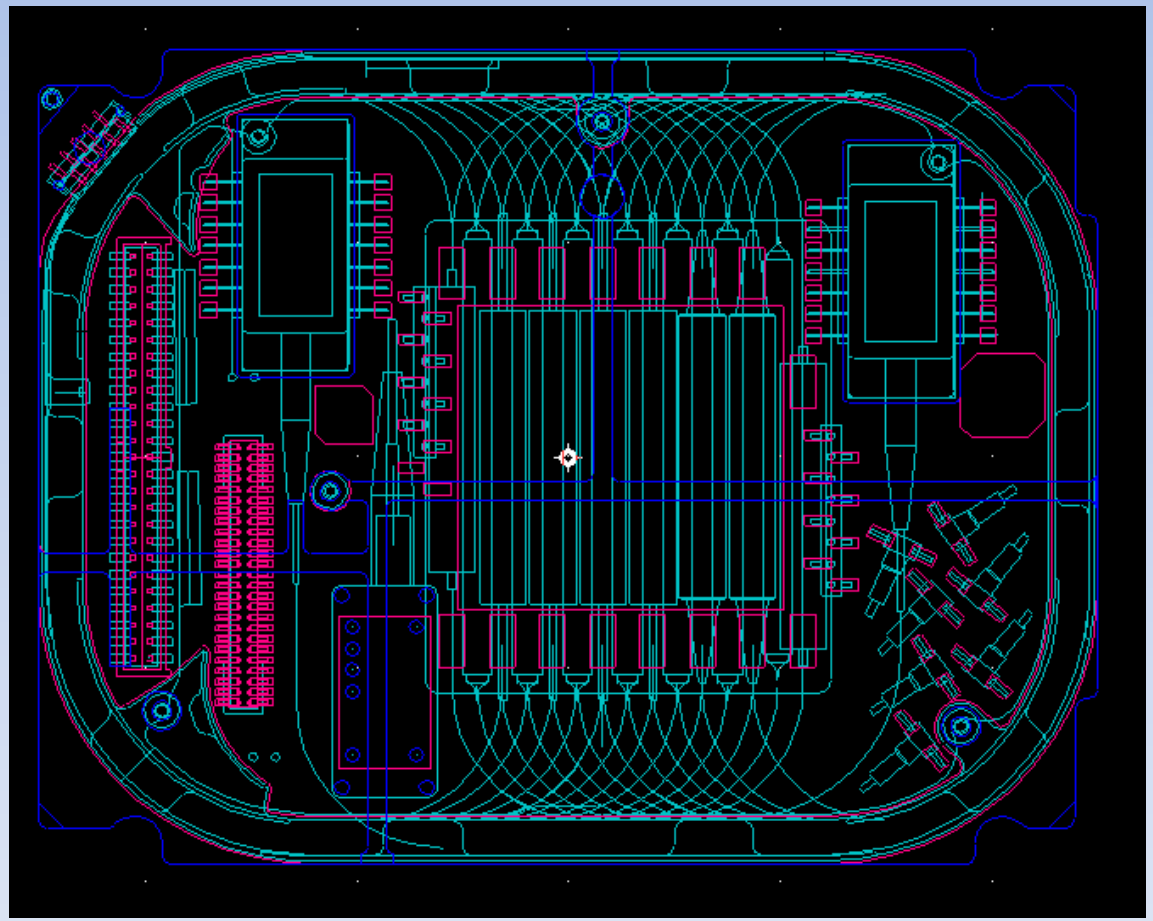
PCB Netlist Verification

The netlist is imported into the pcb database. If all components and connections from the netlist match the pcb database of library components, they will appear as pictured below. Green indicates all components (*part*), yellow indicates connections (*net*) to the components.



Mechanical Inputs

Mechanical placement strategies are imported into the pcb database in the form of a DXF.



PCB Design Requirements

The following requirements and specifications are established prior to pcb layout.

- Customer Specification
- Electrical Requirements
- Mechanical Requirements
- Optical or Data Requirements
- IPC Requirements
- Packaging Requirements
- UL, IEEE, Belcore, Telcordia

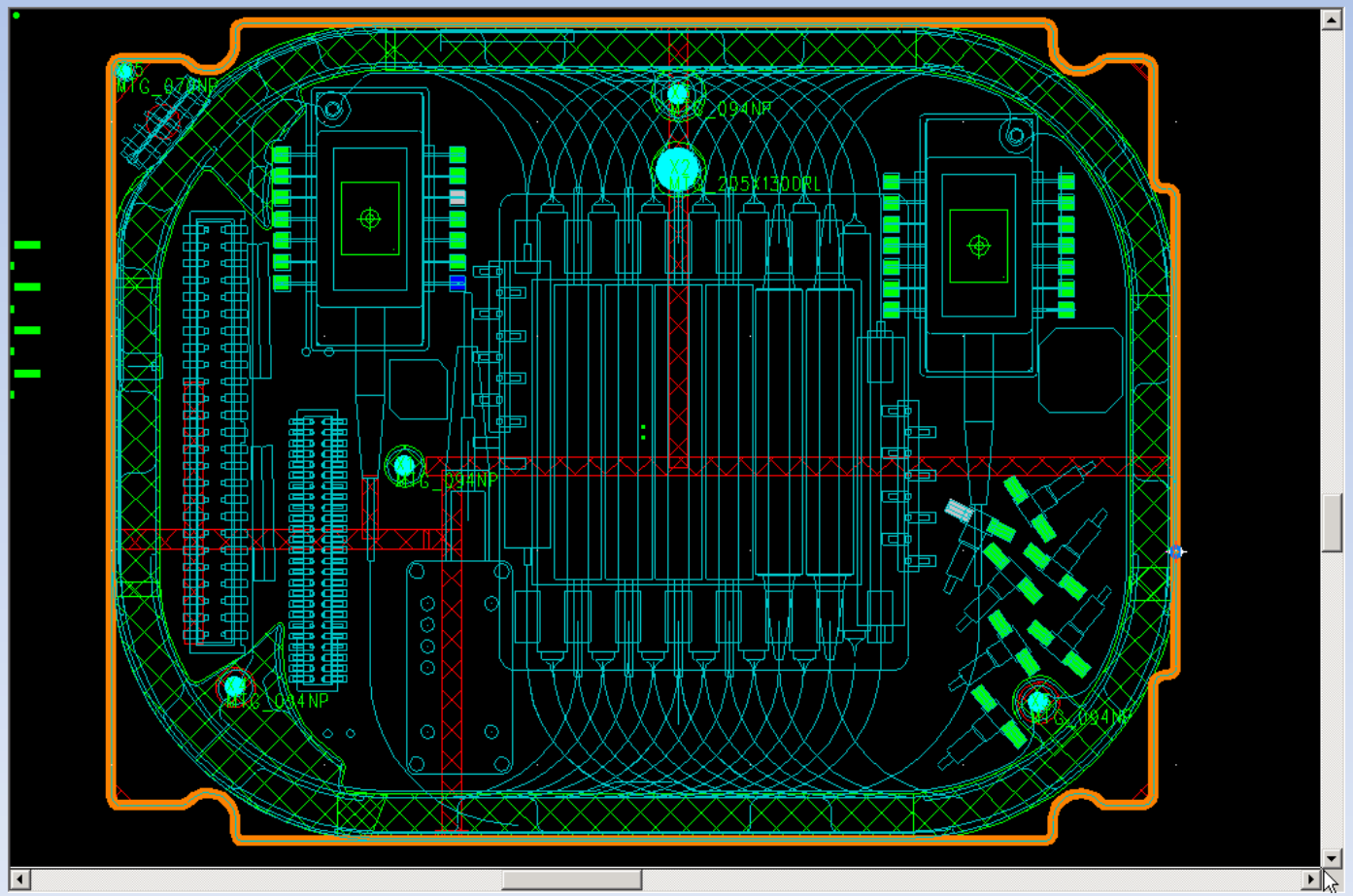
PCB Design Elements

The process and strategies used to design the pcb are typically executed in the order outlined below.

- Import any Mechanical Constraints (DXF)
- Create the Board Outline
- Create Cutouts and Keepouts
- Place Component and Hardware Holes
- Configure PCB Design Rules, Constraints and Preferences
- Define Layer Definitions, Vias and Padstacks
- Import the Schematic Netlist
- Place Components
- Route Traces
- Create Copper Pour areas
- Create Copper Planes
- Define and Implement Test Strategy
- Implement Design Rules Check and Verification
- Orient Silkscreen Reference Designators and Text
- Orient Assembly Drawing Reference Designators and Text
- Dimension PCB and Define Fabrication Drawing
- Create Assembly and Fabrication Drawings
- Build and Generate Gerber and Drill Files PCB Fabrication

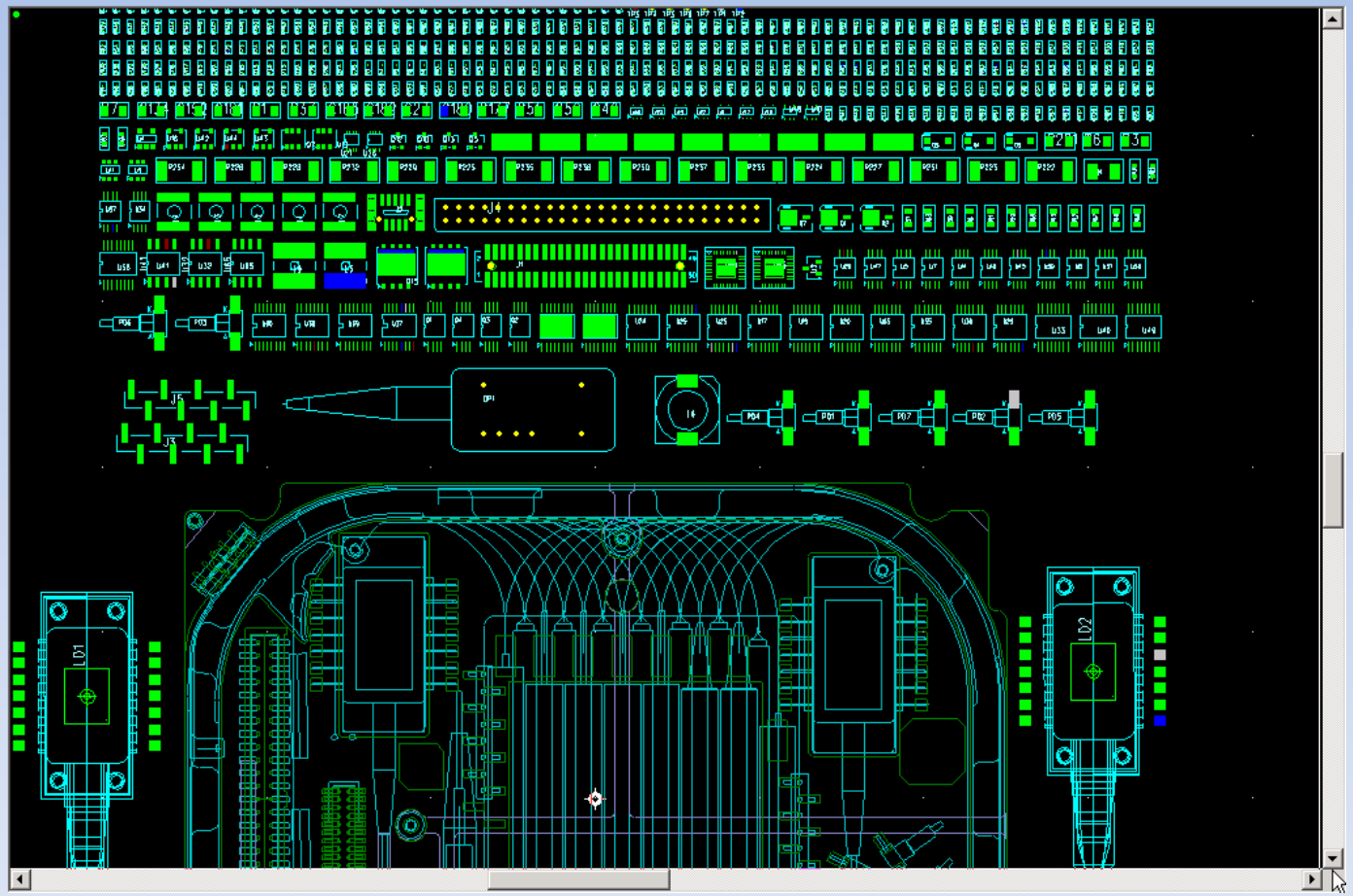
PCB Design: Keepouts

The silkscreen dxf is imported from the mechanical design (blue).
The board outline is created in the pcb database (orange).
Holes and cutouts are manually added (filled cyan circles).
Keepout areas are created (green and red cross-hatched areas).



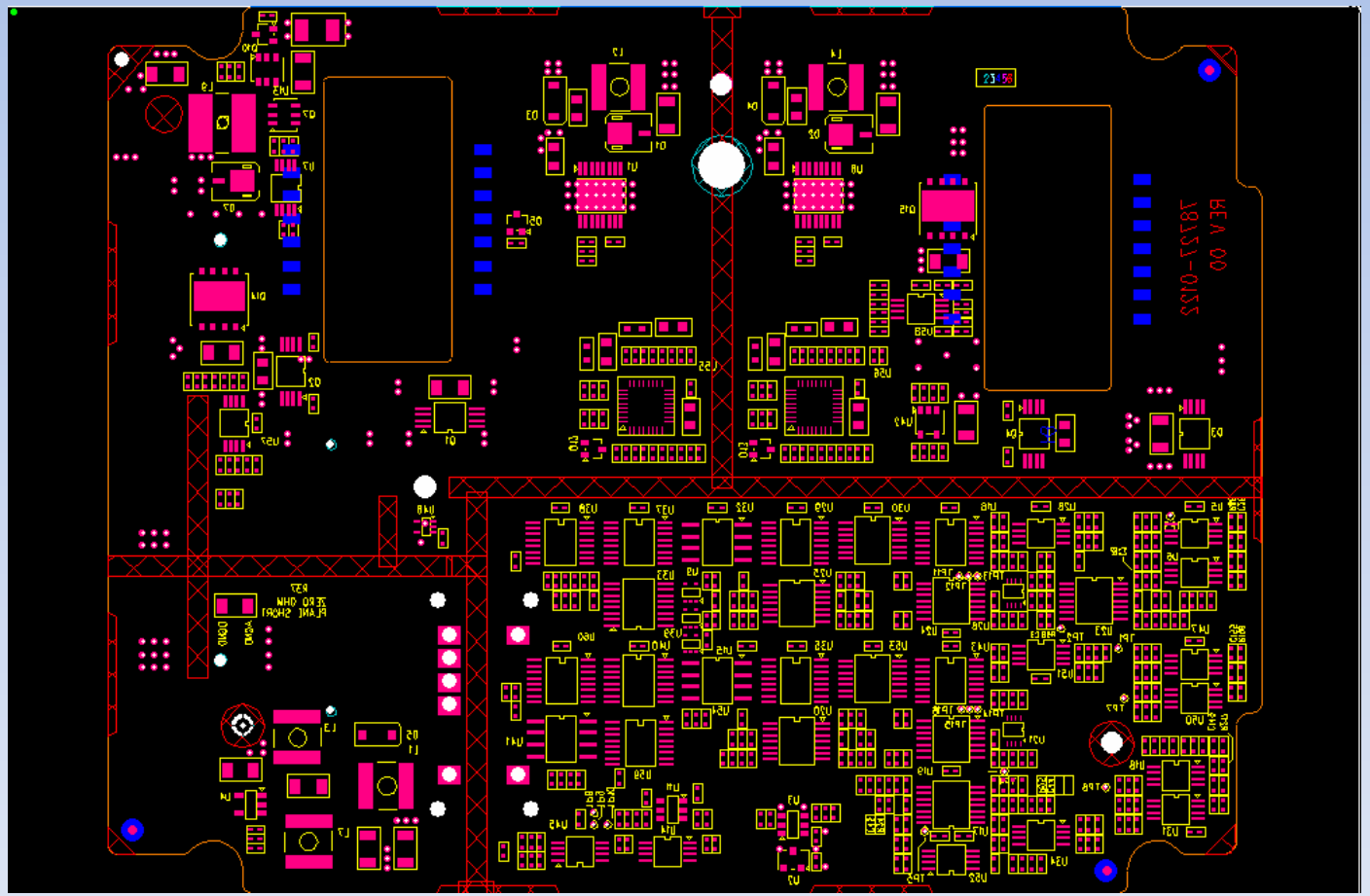
PCB Design: Components

Components from the netlist are dispersed and grouped according to function. The components are then manually placed inside the pcb outline.



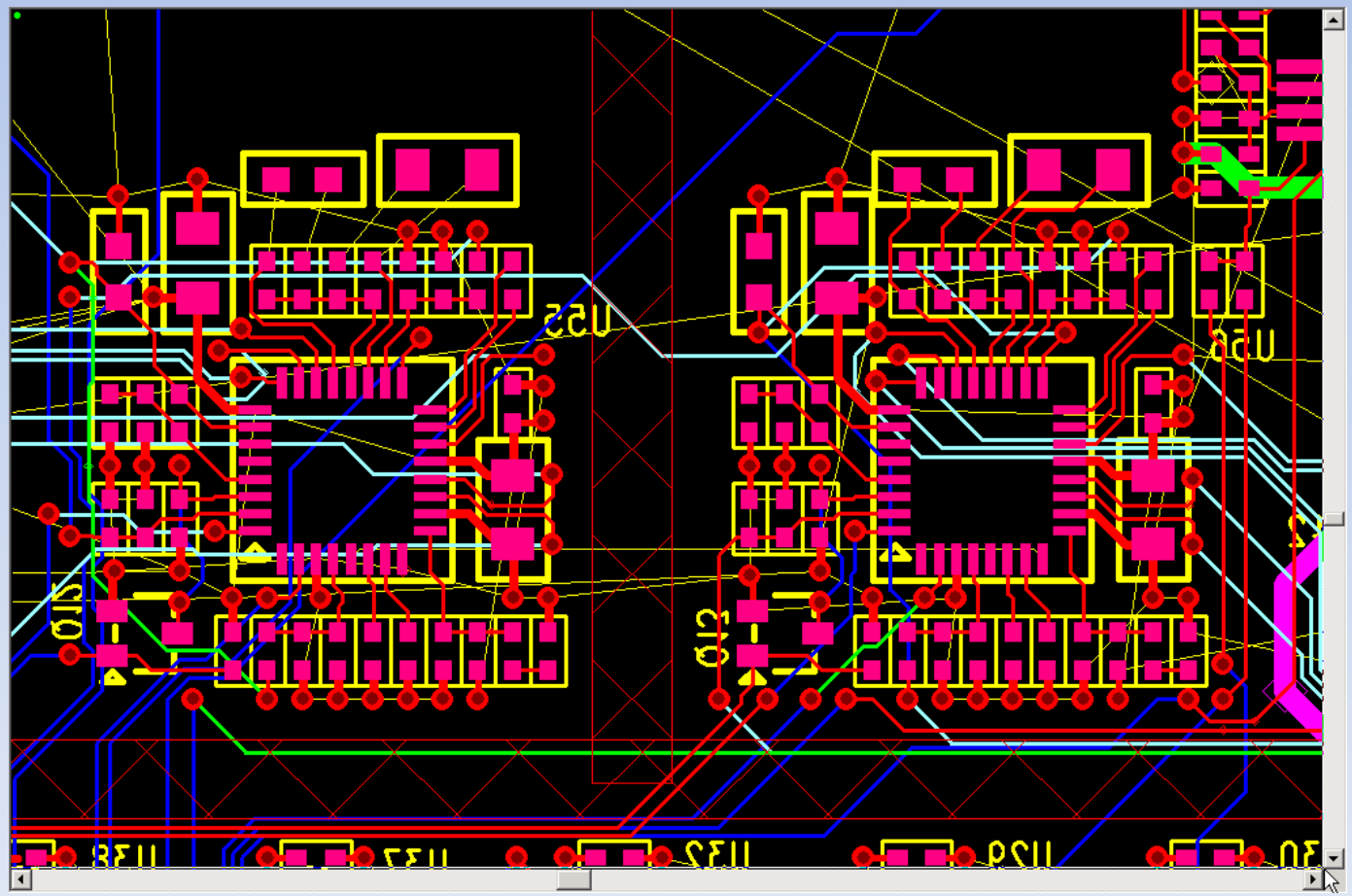
PCB Design: Placement

Components are placed within the pcb board outline.
Keepouts, cutouts and holes must be avoided.



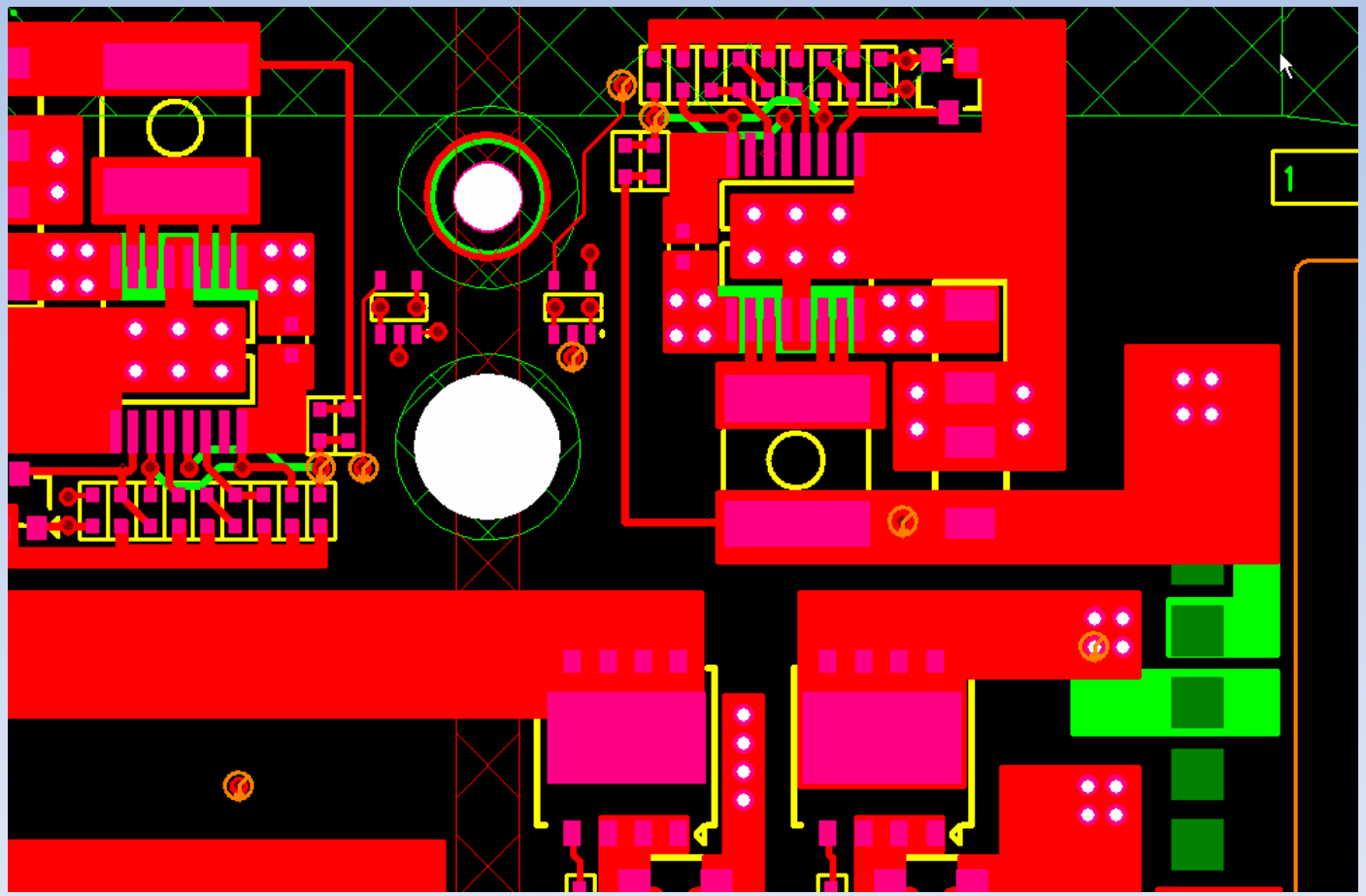
PCB Design: Routing

All connections (nets) require trace routing.
The red lines are completed trace connections.
The yellow lines represent unrouted traces or nets.
Plane connections are created with a via or direct connection to a copper area.
Trace routing may consist of component to component or component to plane connections.



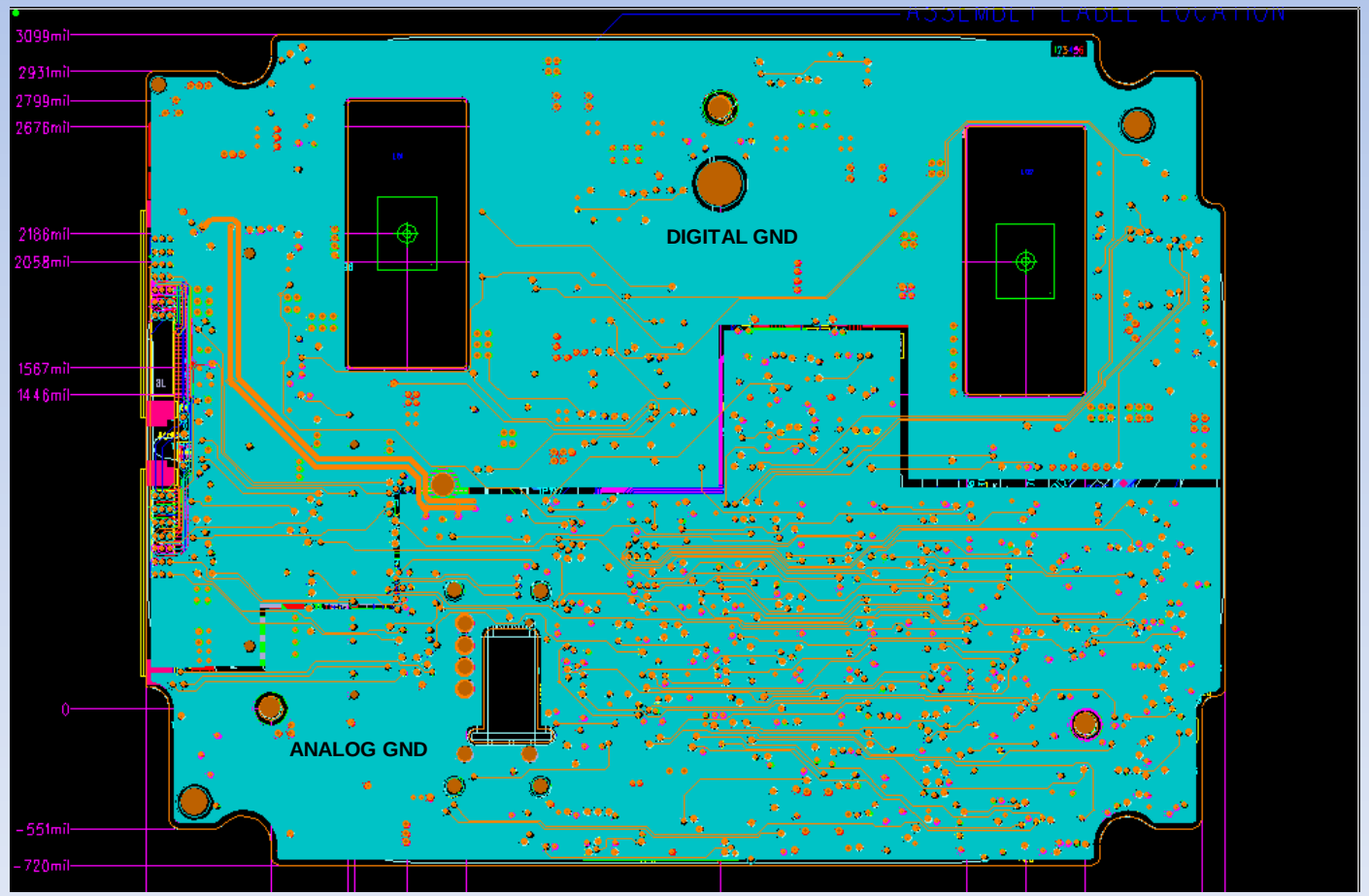
PCB Design: Copper

Copper areas are created (red) and poured over vias (white circles) and solder pads (violet). Copper areas are then assigned a net name that matches with the appropriate net connection.



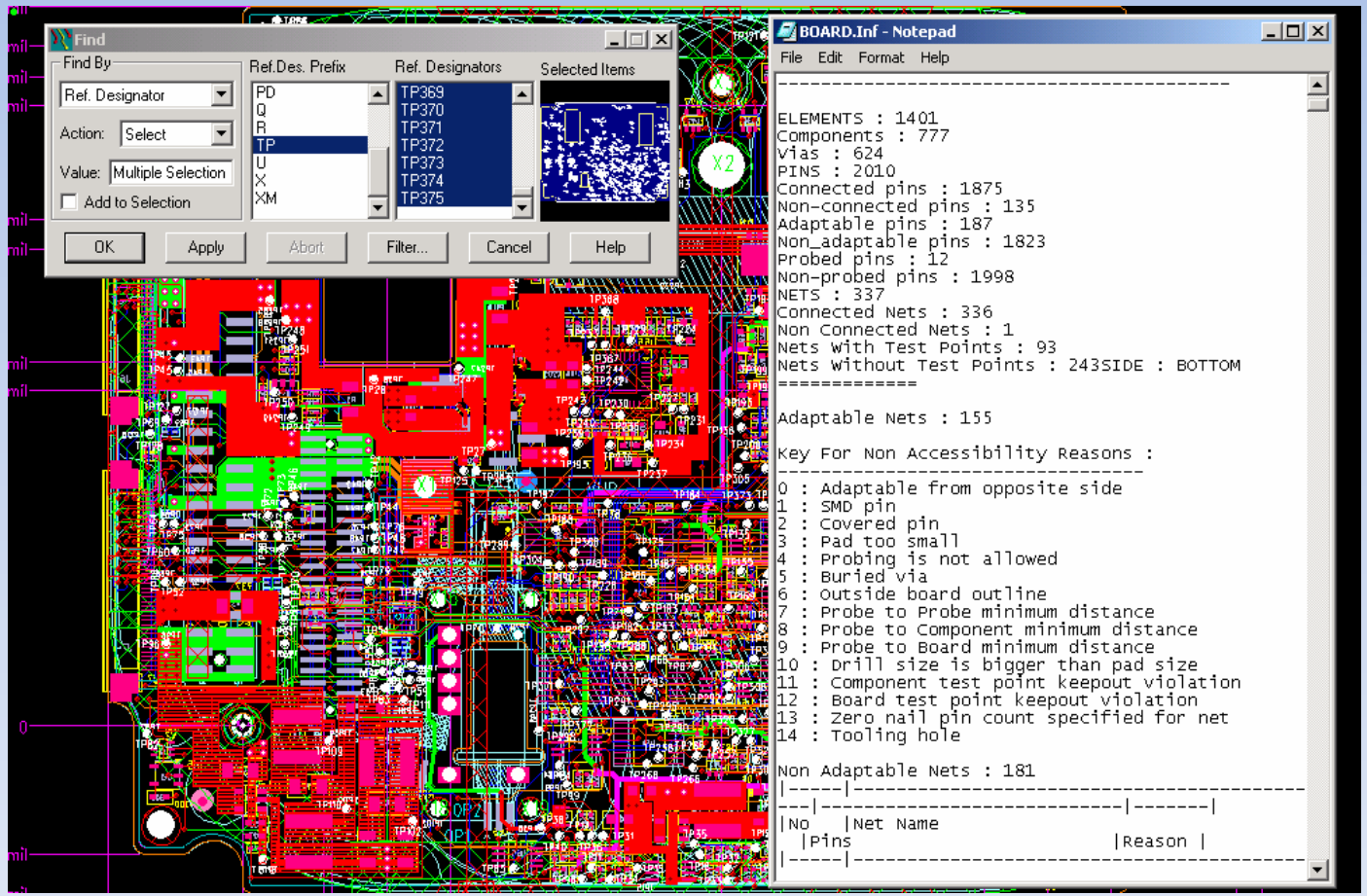
PCB Design: Plane

The copper planes are created, split and defined according to the design rules and net requirements for each layer. Thermal and non-thermal connections are placed accordingly.



PCB Design: DFT

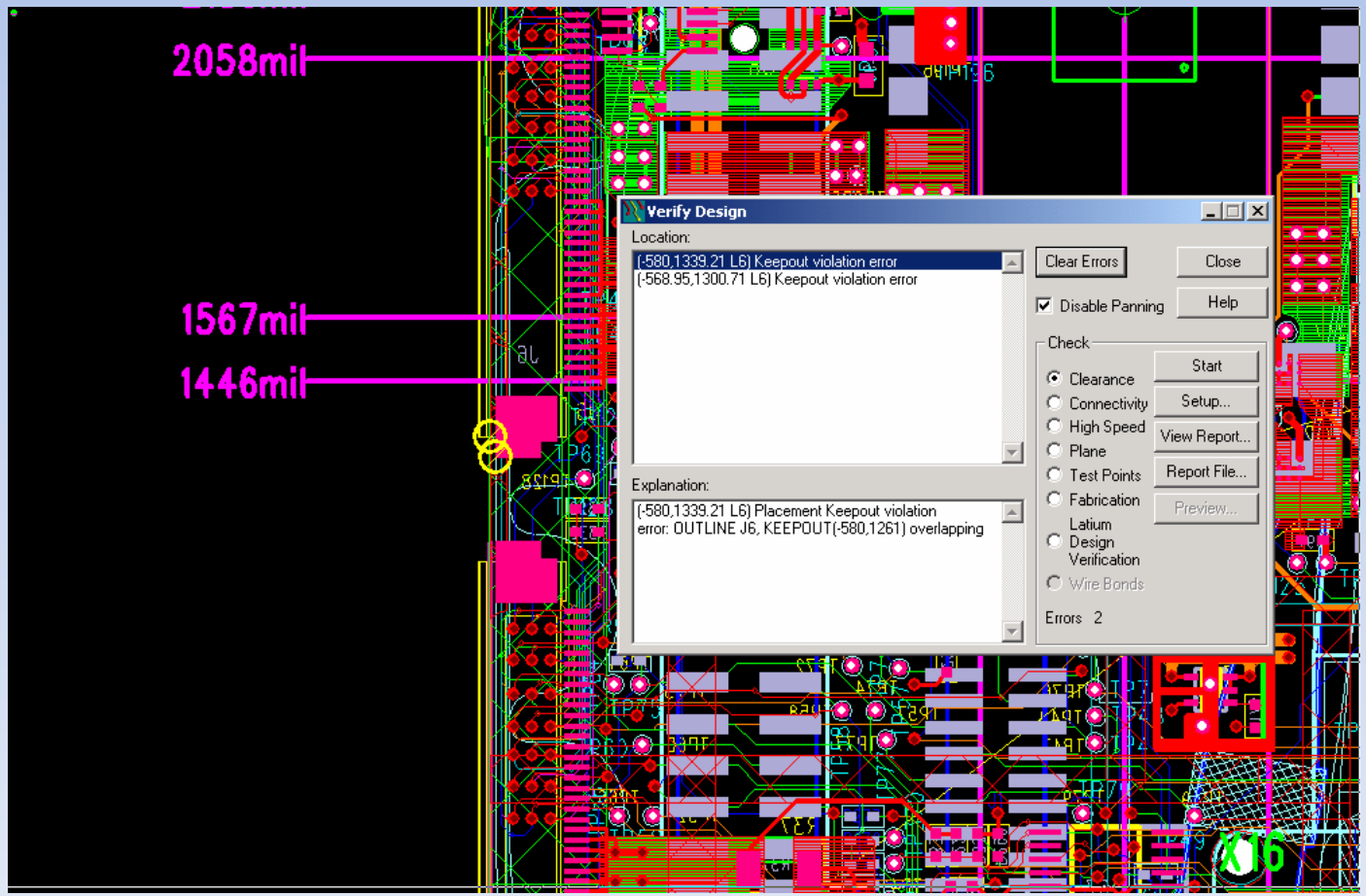
Design for Test involves placement of test points into the completed pcb.
Two types of test points are used. Flying Probe (FPT) and In Circuit (ICT).
DFT analysis is executed and test points are audited for compliance and testability.



PCB Design: Verification

The pcb is complete and must be verified for design rules compliance. Verification includes clearance checks, net and copper connectivity, net and copper plane connectivity, duplicate nets, layer to layer connectivity, design rule violations, DFM and test points.

In this example, the yellow circles indicate a clearance violation (copper to board edge).



Gerber Files

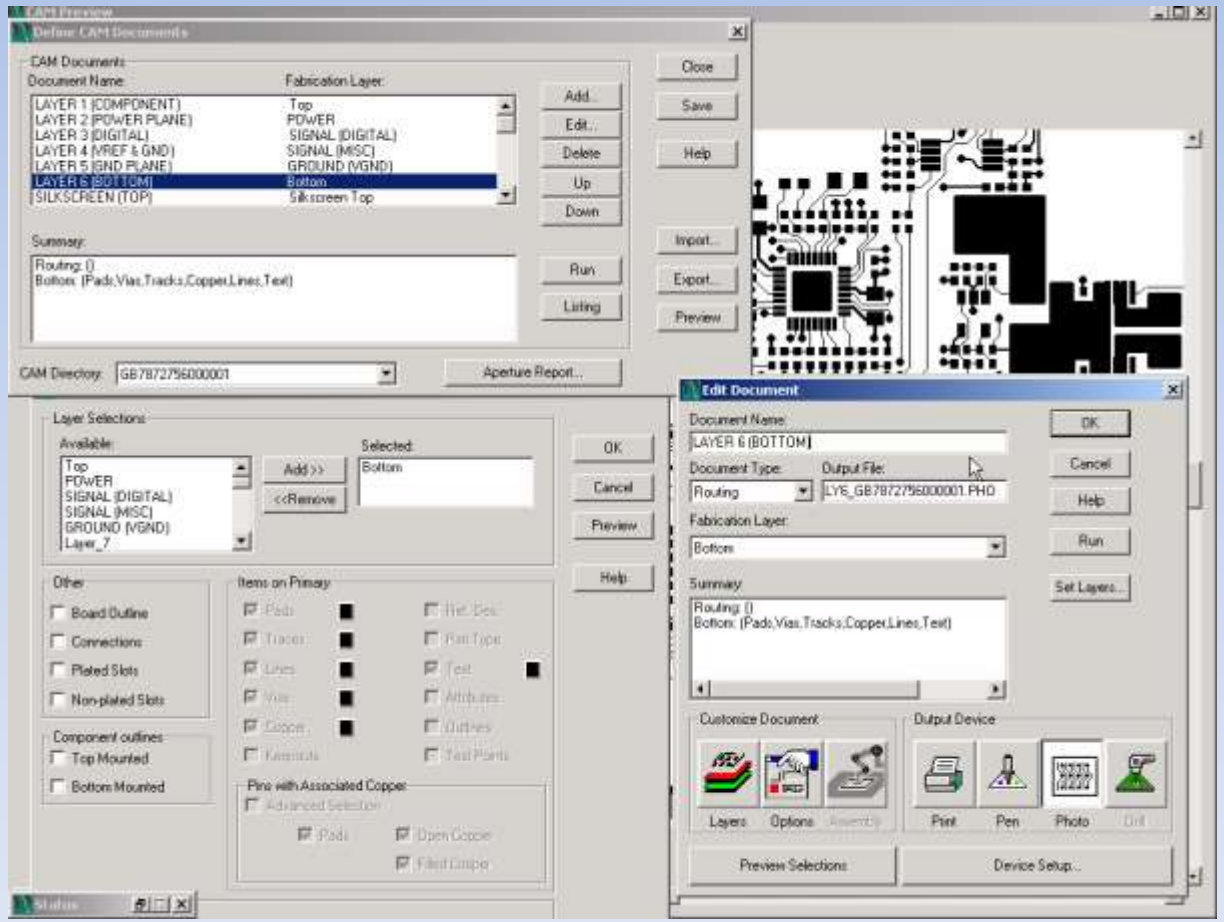
Gerber files are created to enable plotting of the individual design file elements. Depending on their function, each Gerber file is compiled as an individual electrical layer, process or design reference.

Typical Gerber File Structure

- Electrical Design Layers
- Silkscreen
- Solder Mask
- Solder Paste
- Fabrication Drawings
- Assembly Drawings
- Aperture Files
- Drill Files
- Netlist
- X-Y Placement Data

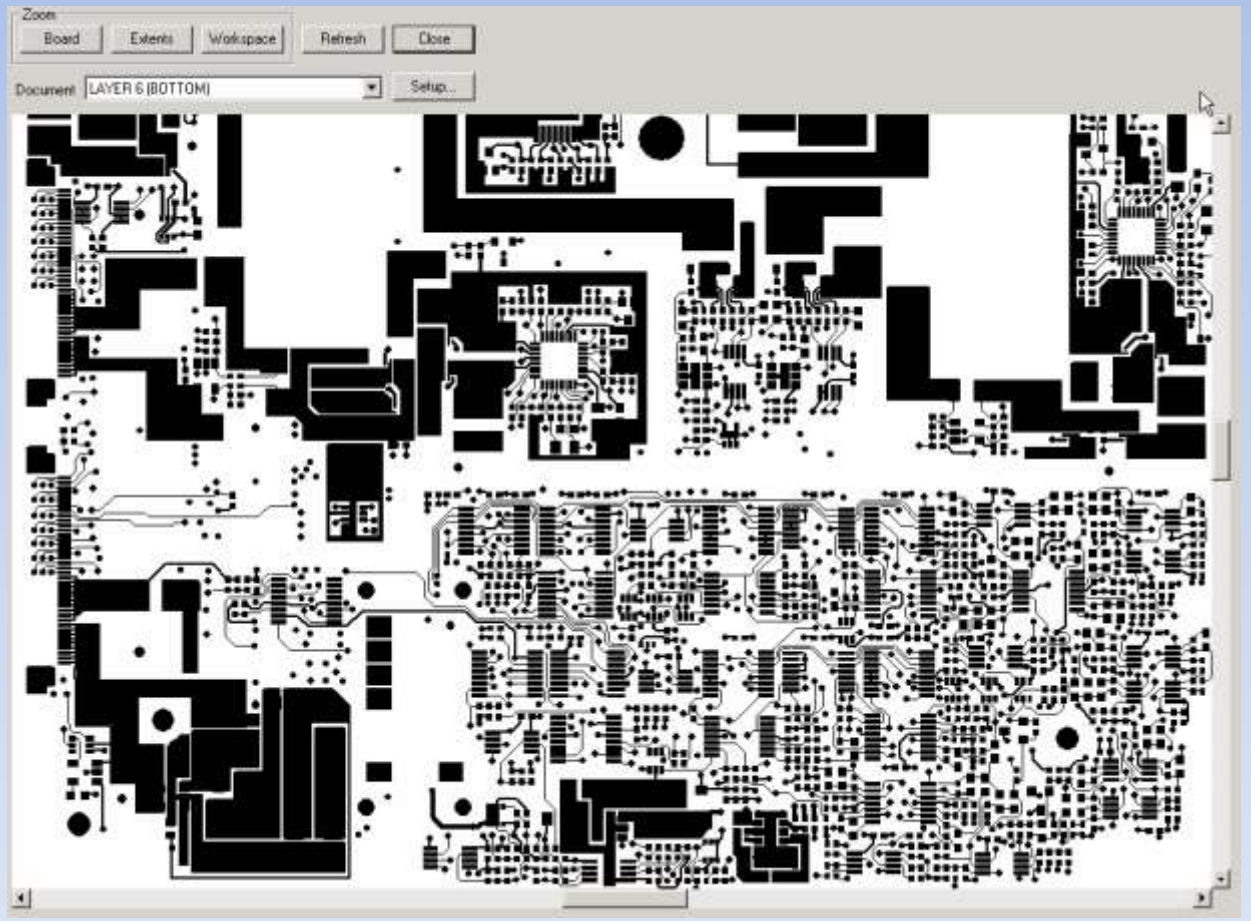
Gerber Files

This is a typical Gerber file design menu. From this menu, design data can be manipulated to any number of conditions to achieve the desired results.



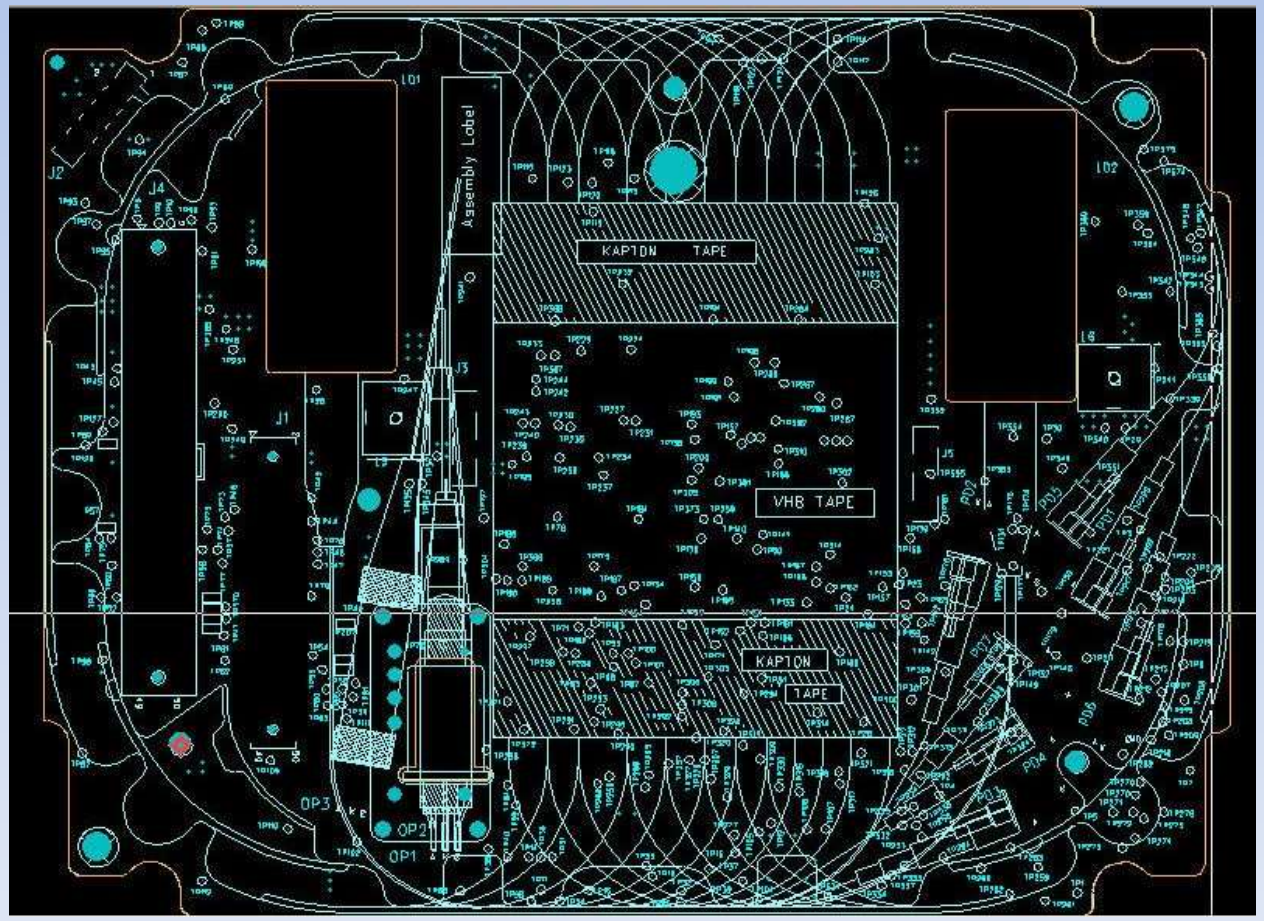
Gerber Files: Electrical Layers

These Gerber files are processed to create each electrical layer (internal and external) that will ultimately be finished in copper on the pcb.



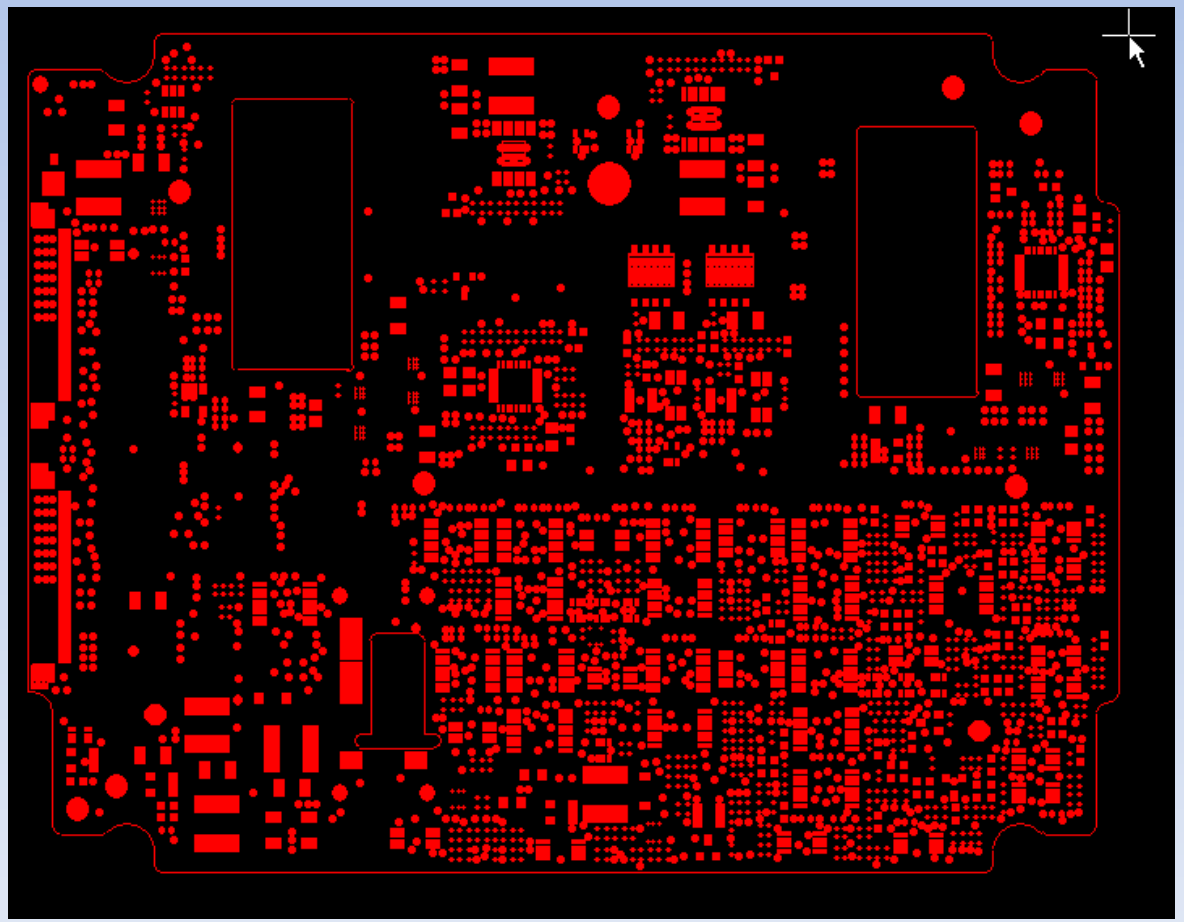
Gerber Files: Silkscreen

This file will create the stencil that will be used to apply the silkscreen (ink) to the pcb.
The Silkscreen is for component reference, identification and labeling.
The Silkscreen exists on the outer layers.



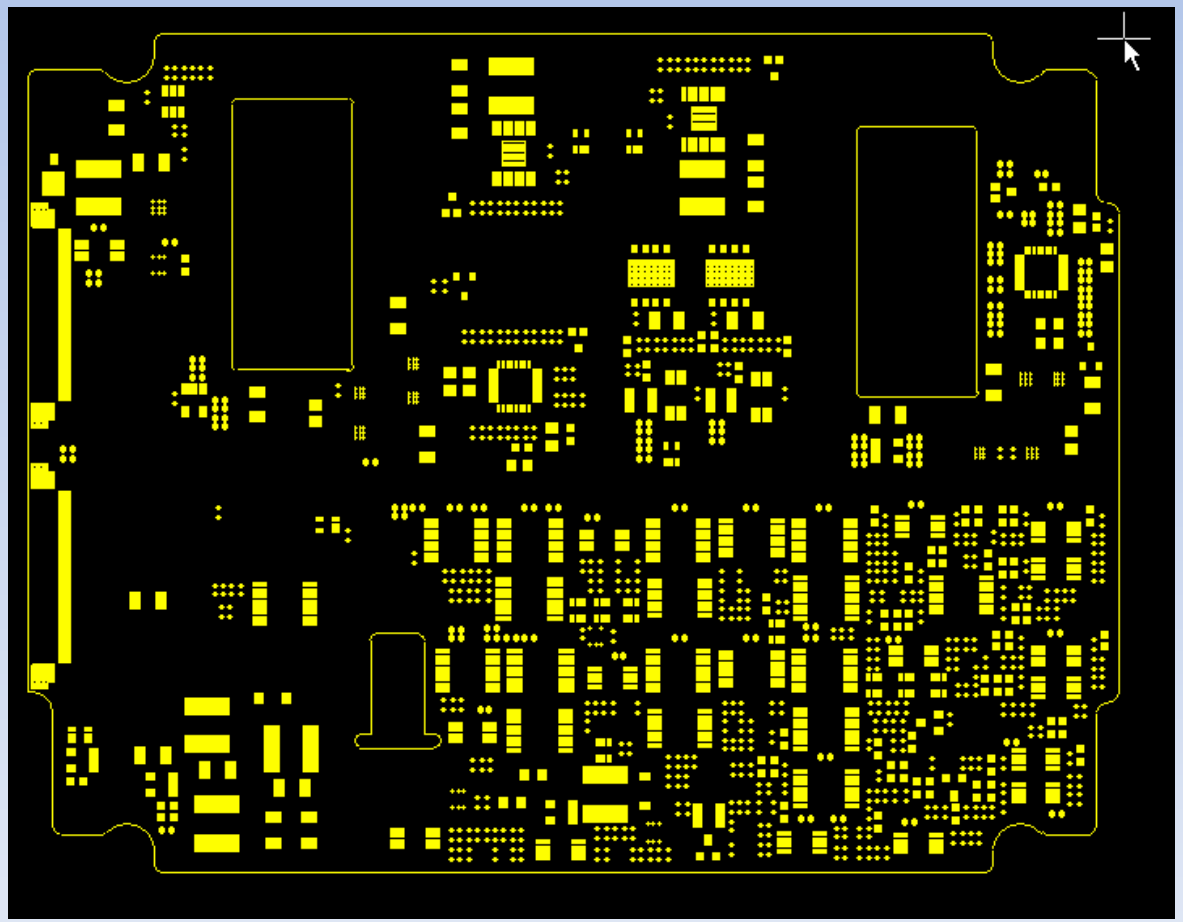
Gerber Files: Solder Mask

The solder mask will expose solderable areas and protect the pcb by covering all copper elements. The Solder Mask minimizes solder bridges.
In this example, the Gerber file was created as a negative. Areas in red will not be covered with mask. The solder mask exists on the outer layers.



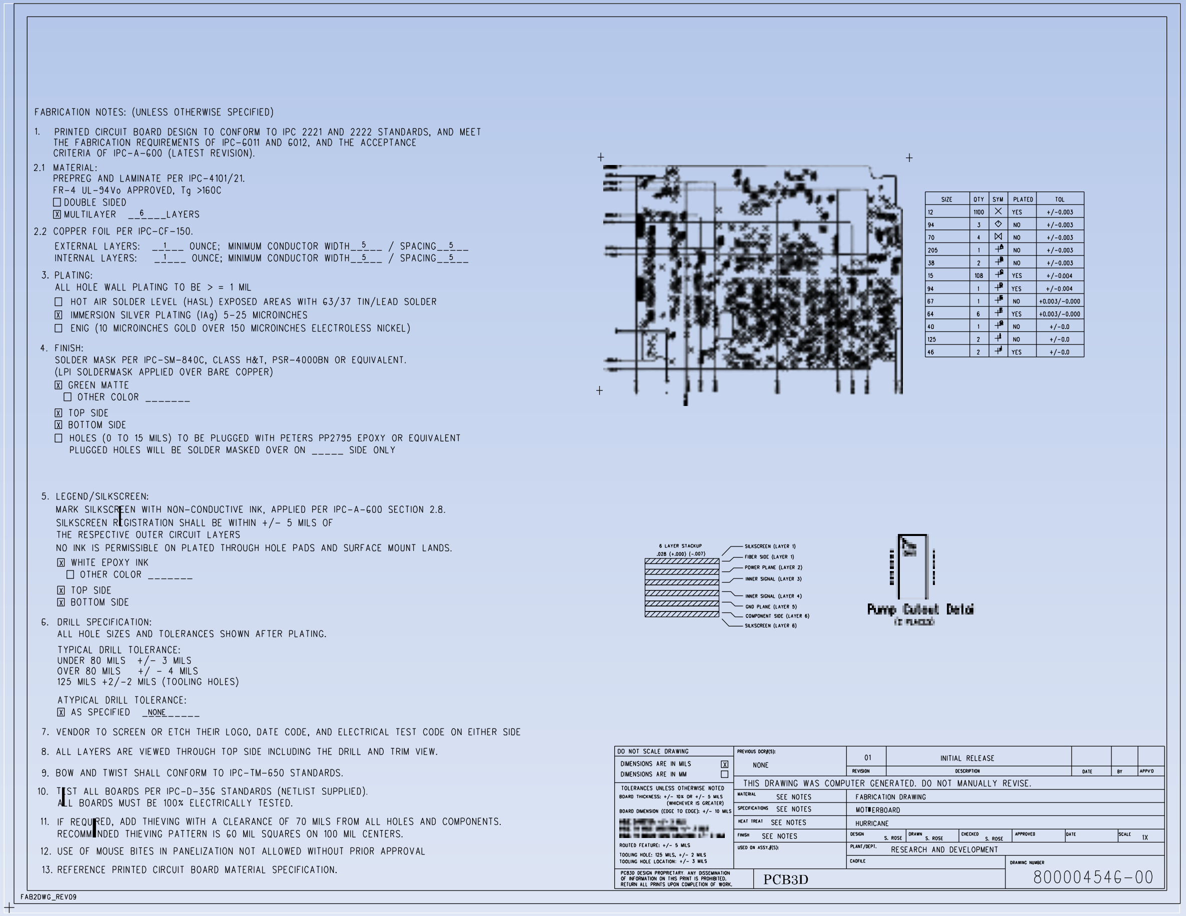
Gerber Files: Solder Paste

This file will be used to create a solder paste stencil. Prior to the board assembly, the stencil will be used to apply solder paste directly to the pads on the pcb (areas in yellow). Once the solder paste is applied, surface mount components can be placed and soldered.



Gerber Files: Fabrication Drawing

This file will be created to display all mechanical and fabrication design parameters of the pcb. Parameters include layer stackup, board thickness, tolerance, drill file, copper weight, dimensioning, and applicable design standards .

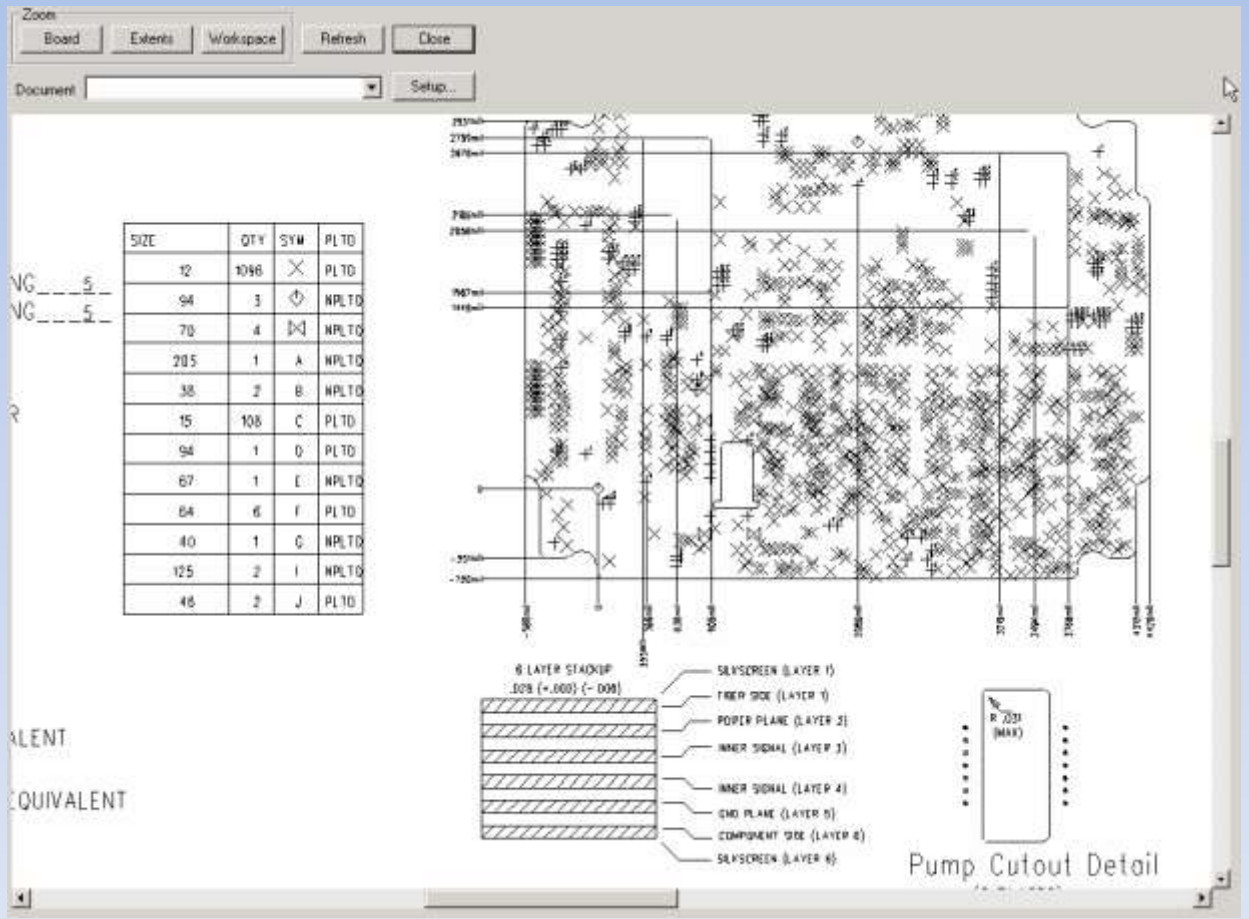


FABRICATION NOTES: (UNLESS OTHERWISE SPECIFIED)
1. PRINTED CIRCUIT BOARD DESIGN TO CONFORM TO IPC 2221 AND 2222 STANDARDS, AND MEET THE FABRICATION REQUIREMENTS OF IPC-6011 AND 6012, AND THE ACCEPTANCE CRITERIA OF IPC-A-600 (LATEST REVISION).
2.1 MATERIAL:
PREPREG AND LAMINATE PER IPC-4101/21.
FR-4 UL-94Vo APPROVED, Tg >160C
☐ DOUBLE SIDED
☒ MULTILAYER __6____LAYERS
2.2 COPPER FOIL PER IPC-CF-150.
EXTERNAL LAYERS: __1___ OUNCE; MINIMUM CONDUCTOR WIDTH__5___ / SPACING__5___
INTERNAL LAYERS: __1___ OUNCE; MINIMUM CONDUCTOR WIDTH__5___ / SPACING__5___
3. PLATING:
ALL HOLE WALL PLATING TO BE > = 1 MIL
☐ HOT AIR SOLDER LEVEL (HASL) EXPOSED AREAS WITH 63/37 TIN/LEAD SOLDER
☒ IMMERSION SILVER PLATING (IAg) 5-25 MICROINCHES
☐ ENIG (10 MICROINCHES GOLD OVER 150 MICROINCHES ELECTROLESS NICKEL)
4. FINISH:
SOLDER MASK PER IPC-SM-840C, CLASS H&T, PSR-4000BN OR EQUIVALENT.
(LPI SOLDERMASK APPLIED OVER BARE COPPER)
☒ GREEN MATTE
☐ OTHER COLOR _______
☒ TOP SIDE
☒ BOTTOM SIDE
☐ HOLES (0 TO 15 MILS) TO BE PLUGGED WITH PETERS PP2795 EPOXY OR EQUIVALENT
PLUGGED HOLES WILL BE SOLDER MASKED OVER ON _____ SIDE ONLY
5. LEGEND/SILKSCREEN:
MARK SILKSCREEN WITH NON-CONDUCTIVE INK, APPLIED PER IPC-A-600 SECTION 2.8.
SILKSCREEN REGISTRATION SHALL BE WITHIN +/- 5 MILS OF
THE RESPECTIVE OUTER CIRCUIT LAYERS
NO INK IS PERMISSIBLE ON PLATED THROUGH HOLE PADS AND SURFACE MOUNT LANDS.
☒ WHITE EPOXY INK
☐ OTHER COLOR _______
☒ TOP SIDE
☒ BOTTOM SIDE
6. DRILL SPECIFICATION:
ALL HOLE SIZES AND TOLERANCES SHOWN AFTER PLATING.
TYPICAL DRILL TOLERANCE:
UNDER 80 MILS +/- 3 MILS
OVER 80 MILS +/ - 4 MILS
125 MILS +2/-2 MILS (TOOLING HOLES)
ATYPICAL DRILL TOLERANCE:
☒ AS SPECIFIED _NONE_____
7. VENDOR TO SCREEN OR ETCH THEIR LOGO, DATE CODE, AND ELECTRICAL TEST CODE ON EITHER SIDE
8. ALL LAYERS ARE VIEWED THROUGH TOP SIDE INCLUDING THE DRILL AND TRIM VIEW.
9. BOW AND TWIST SHALL CONFORM TO IPC-TM-650 STANDARDS.
10. TEST ALL BOARDS PER IPC-D-356 STANDARDS (NETLIST SUPPLIED).
ALL BOARDS MUST BE 100% ELECTRICALLY TESTED.
11. IF REQUIRED, ADD THIEVING WITH A CLEARANCE OF 70 MILS FROM ALL HOLES AND COMPONENTS.
RECOMMENDED THIEVING PATTERN IS 60 MIL SQUARES ON 100 MIL CENTERS.
12. USE OF MOUSE BITES IN PANELIZATION NOT ALLOWED WITHOUT PRIOR APPROVAL
13. REFERENCE PRINTED CIRCUIT BOARD MATERIAL SPECIFICATION.
6 LAYER STACKUP
.028 (+.000) (-.007)
SILKSCREEN (LAYER 1)
FIBER SIDE (LAYER 1)
POWER PLANE (LAYER 2)
INNER SIGNAL (LAYER 3)
INNER SIGNAL (LAYER 4)
GND PLANE (LAYER 5)
COMPONENT SIDE (LAYER 6)
SILKSCREEN (LAYER 6)
DO NOT SCALE DRAWING
DIMENSIONS ARE IN MILS ☒
DIMENSIONS ARE IN MM ☐
TOLERANCES UNLESS OTHERWISE NOTED
BOARD THICKNESS: +/- 10% OR +/- 5 MILS (WHICHEVER IS GREATER)
BOARD DIMENSION (EDGE TO EDGE): +/- 10 MILS
ROUTED FEATURE: +/- 5 MILS
TOOLING HOLE: 125 MILS, +/- 2 MILS
TOOLING HOLE LOCATION: +/- 3 MILS
PCB3D DESIGN PROPRIETARY. ANY DISSEMINATION OF INFORMATION ON THIS PRINT IS PROHIBITED. RETURN ALL PRINTS UPON COMPLETION OF WORK.
PREVIOUS DCR#(S): NONE
REVISION 01
DESCRIPTION INITIAL RELEASE
DATE
BY
APPV'D
THIS DRAWING WAS COMPUTER GENERATED. DO NOT MANUALLY REVISE.
MATERIAL SEE NOTES
SPECIFICATIONS SEE NOTES
HEAT TREAT SEE NOTES
FINISH SEE NOTES
USED ON ASSY.#(S):
FABRICATION DRAWING
MOTHERBOARD
HURRICANE
DESIGN S. ROSE
DRAWN S. ROSE
CHECKED S. ROSE
APPROVED
DATE
SCALE 1X
PLANT/DEPT. RESEARCH AND DEVELOPMENT
CADFILE
DRAWING NUMBER 800004546-00
PCB3D
FAB2DWG_REV09

SIZE	QTY	SYM	PLATED	TOL
12	1100	X	YES	+/-0.003
94	3	◇	NO	+/-0.003
70	4	⋈	NO	+/-0.003
205	1	+A	NO	+/-0.003
38	2	+B	NO	+/-0.003
15	108	+C	YES	+/-0.004
94	1	+D	YES	+/-0.004
67	1	+E	NO	+0.003/-0.000
64	6	+F	YES	+0.003/-0.000
40	1	+G	NO	+/-0.0
125	2	+I	NO	+/-0.0
46	2	+J	YES	+/-0.0

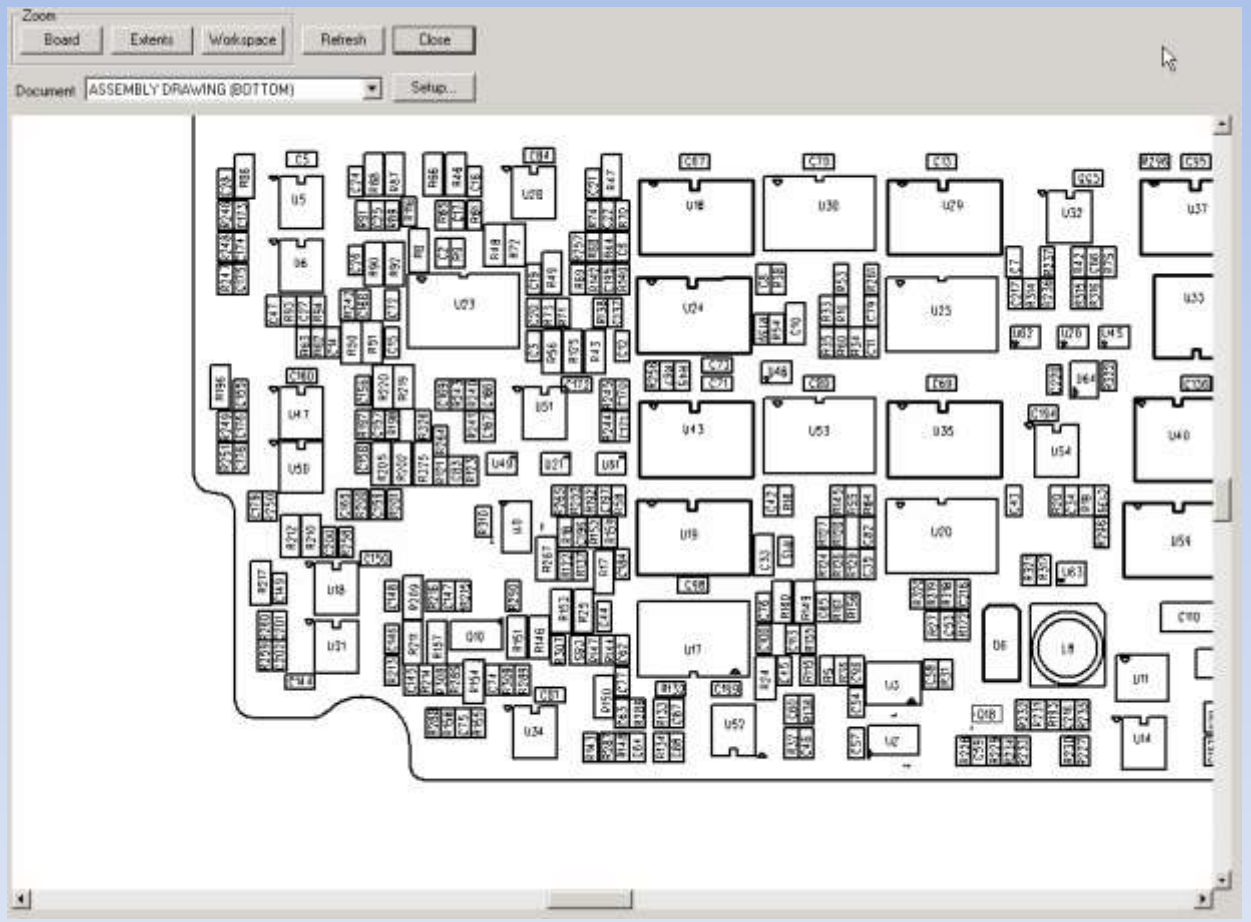
Gerber Files: Fabrication Details

Pcb manufacturing details include drill size, plating, drill location information, electrical layer stackup, board thickness, slots, cutouts and tolerance.



Gerber Files: Assembly Drawing

Identifies location and orientation of the electronic components to be placed.



Gerber Files: Aperture Listing

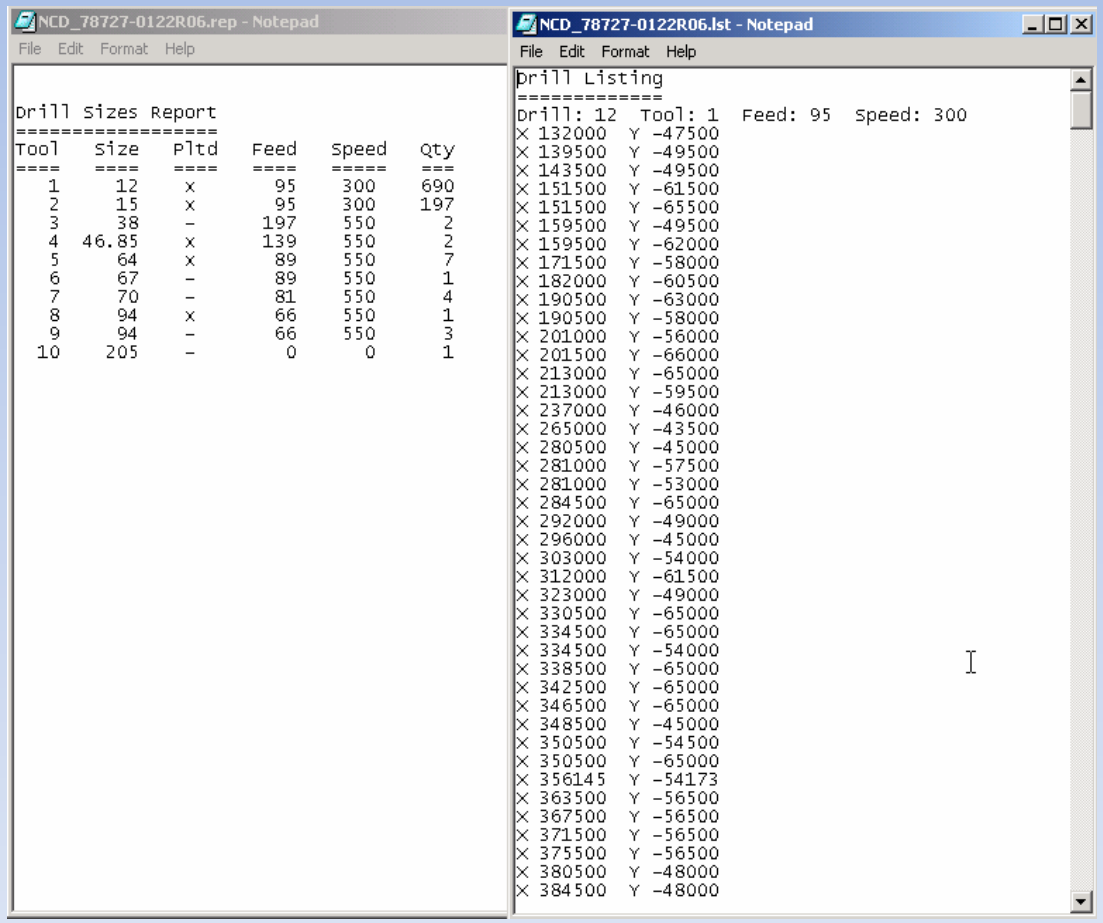
This listing defines the shape of individual elements on the pcb.

Photo-Plotter Apertures Report

Position	Width	Hgt/ID	Shape	Qty
10	25	0	RND	292
11	20	0	RND	65
12	10	0	RND	3606
13	7	0	RND	61
14	5	0	RND	34500
15	1	0	RND	2
16	8	0	RND	4011
18	94	0	RND	8
21	70	0	RND	16
25	45	70	RECT	28
27	30	0	RND	916
28	50	0	SQR	38
35	40	0	SQR	32
48	12	0	RND	197
49	15	0	RND	40
51	35	0	RND	197
54	18	0	RND	37
59	3	0	RND	1202
60	100	0	RND	4
68	75	0	RND	8
74	55	0	SQR	28
75	105	0	SQR	1
78	34	0	SQR	50
79	25	0	SQR	46
80	35	0	SQR	1
89	0.5	0	RND	58
90	4	0	RND	641
92	6	0	RND	48
106	30	0	SQR	26
111	31	0	SQR	10
112	40.16	0	SQR	100
114	27.56	0	SQR	24
115	15.75	0	SQR	386
116	18	0	SQR	272
120	27	0	SQR	36
121	100	0	SQR	2
122	85	0	SQR	14
125	45	0	SQR	64
133	33	0	SQR	10

Gerber Files: Drill Files

CNC drill parameters used on the pcb fabricators system to drill and route the pcb.



NCD_78727-0122R06.rep - Notepad

File Edit Format Help

```
Drill Sizes Report
==================
Tool    Size    Pltd    Feed    Speed    Qty
====    ====    ====    ====    =====    ===
   1      12       x      95      300    690
   2      15       x      95      300    197
   3      38       -     197      550      2
   4   46.85       x     139      550      2
   5      64       x      89      550      7
   6      67       -      89      550      1
   7      70       -      81      550      4
   8      94       x      66      550      1
   9      94       -      66      550      3
  10     205       -       0        0      1
```

NCD_78727-0122R06.lst - Notepad

File Edit Format Help

```
Drill Listing
=============
Drill: 12  Tool: 1  Feed: 95  Speed: 300
X 132000  Y -47500
X 139500  Y -49500
X 143500  Y -49500
X 151500  Y -61500
X 151500  Y -65500
X 159500  Y -49500
X 159500  Y -62000
X 171500  Y -58000
X 182000  Y -60500
X 190500  Y -63000
X 190500  Y -58000
X 201000  Y -56000
X 201500  Y -66000
X 213000  Y -65000
X 213000  Y -59500
X 237000  Y -46000
X 265000  Y -43500
X 280500  Y -45000
X 281000  Y -57500
X 281000  Y -53000
X 284500  Y -65000
X 292000  Y -49000
X 296000  Y -45000
X 303000  Y -54000
X 312000  Y -61500
X 323000  Y -49000
X 330500  Y -65000
X 334500  Y -65000
X 334500  Y -54000
X 338500  Y -65000
X 342500  Y -65000
X 346500  Y -65000
X 348500  Y -45000
X 350500  Y -54500
X 350500  Y -65000
X 356145  Y -54173
X 363500  Y -56500
X 367500  Y -56500
X 371500  Y -56500
X 375500  Y -56500
X 380500  Y -48000
X 384500  Y -48000
```

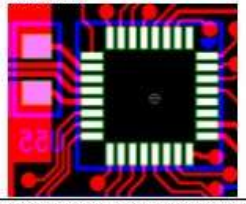
Design Review Process: DFT/DFM

(Preliminary and Final Design Review Audit)

- The Preliminary PCB Design is presented and scrutinized by Manufacturing, Test, Reliability, Electronics and Mechanical Engineering.
- DFM/DFT feedback is reviewed and validated.
- Design Guidelines are reviewed and verified.
- Cost considerations are addressed.
- Manufacturing and assembly process are reviewed.
- A final PCB Design review will present all actions from the Preliminary Design Review.
- Gerber files are analyzed and design intent validated.
- Mechanical and PCB files are overlaid and verified.
- Gerber data files are created.
- The PCB Design is released.

PCB DFT / DFM: Analysis

To ensure a cost effective, robust design, prior to the release of the pcb, the design is sent to the PCB Manufacturer for post-processing feedback.

Ref. No.	DFM Section	Issue/Comments	Impact of Issue: (High / Medium / Low)	Customer Response: (Accept / Reject, Planned Re-spin, Ignore?)
23	7.4.8	It is recommended for 0.5 mm pitch leaded devices to use a 10 mil pad with a consistent space of 9.7 mils. Design uses 12 mil wide pads with a 7.7 mil space. U55 and U56 uses a 12 mil pad width which can contribute to solder shorts. 	Corrected to 10 mils. No issue.	
24	7.4.8	It is recommended for 0.65 mm pitch leaded devices to use a 14 mil pad with consistent spacing of 11.6 mils. The design uses multiple pad widths for 0.65 mm pitch. Recommend changing to 14 mil for consistancy and optimum DPMO results.	All Addressed.	

Design Review Process

(Final Review) Incorporate Design Review Notes and DFT/ DFM Feedback.

Interface Board PCBA Final Design Review.

Attendees: Lori Karl, Steve Rose, Scott Stewart, Lloyd Newfield, John Lodge, Jim McLaren, Jody Baron

1. Confirm final mechanical overlay check with Jody. (Complete)
2. VOA requirements have been removed. (Complete)
3. Scott to contact Fab house regarding modified soldermask opening on 9pin BGA. (Complete)

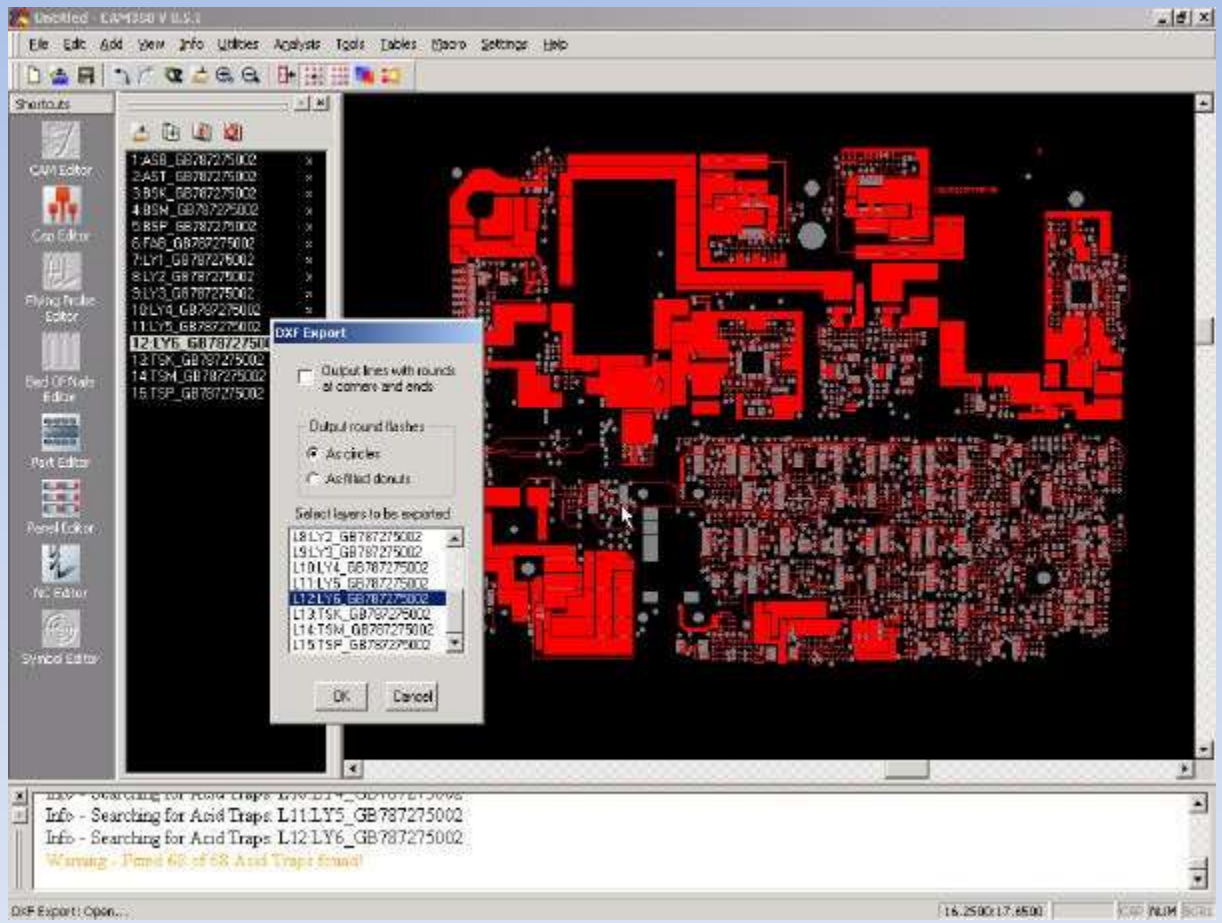
Interface Board PCBA Preliminary Design Review

Attendees: Rich Riddle, Jim McLaren, Scott Stewart, John Mansfield, Steve Rose, Lloyd Newfield, Jody Baron

1. Lloyd to provide part numbers to Rich on EDVT parts which are planned to be NOPOP'ed at assembly, but need to be installed for EDVT testing by Rich's group. Lloyd to provide part numbers and target quantity to Rich.
2. Jody will lower ribs on new base under J7 (flex connector) to prevent shorting base to pads or vias. Rib to be removed under J6. Middle rib will be lowered .040”, to clear pads of J7.

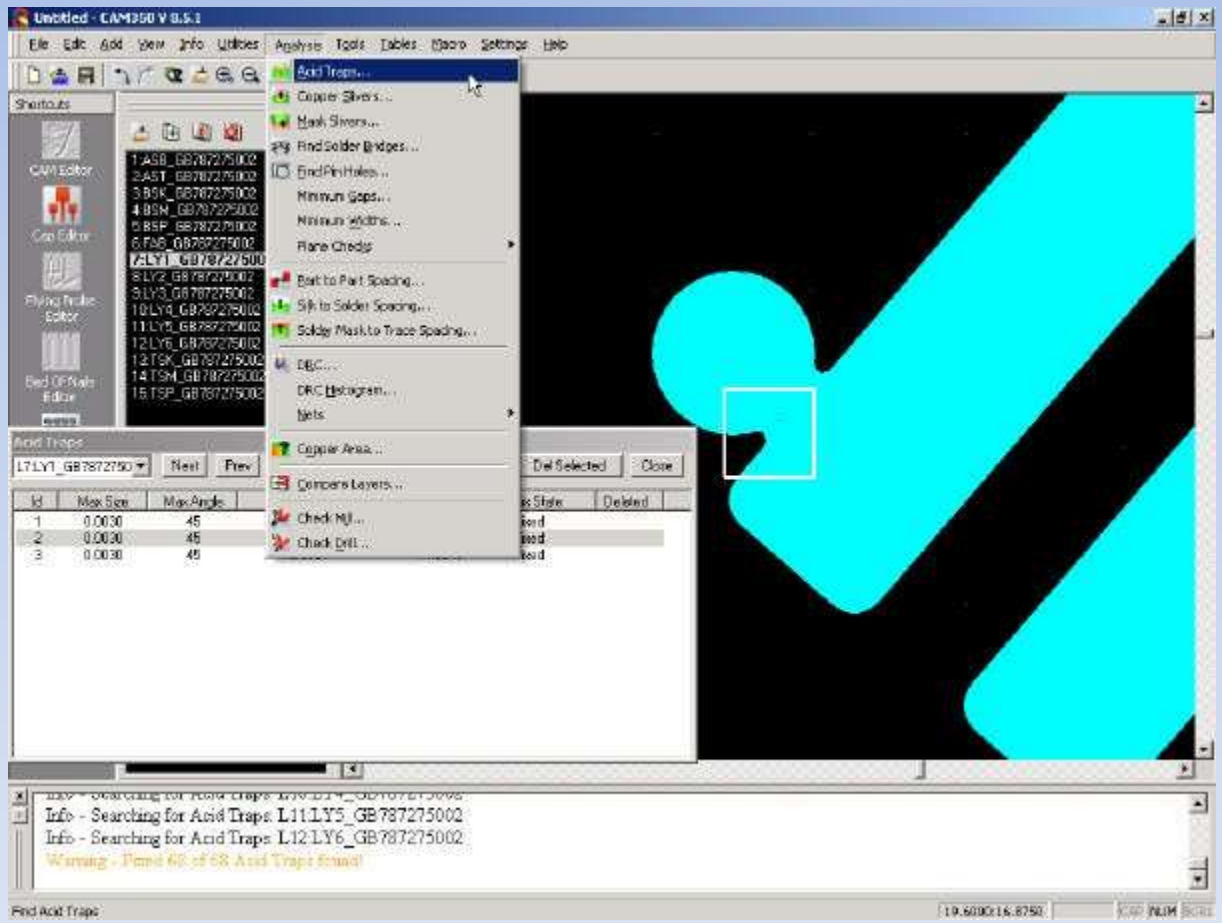
Overlay Output

The Mechanical and PCB database is merged and the design intent is validated.



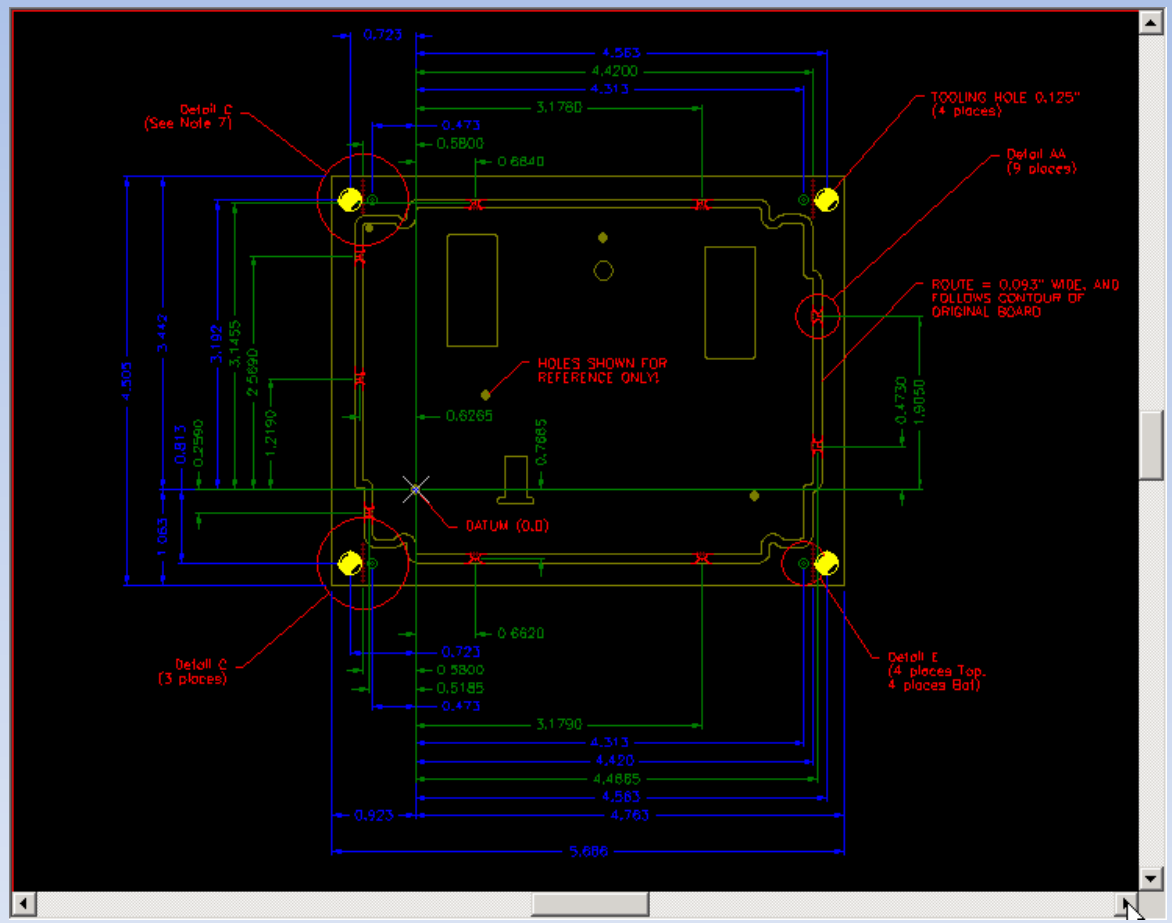
Gerber Analysis and Plotfile Verification

The Gerber files are imported into the Gerber editor for analysis.



PCB DFT / DFM: Panelization

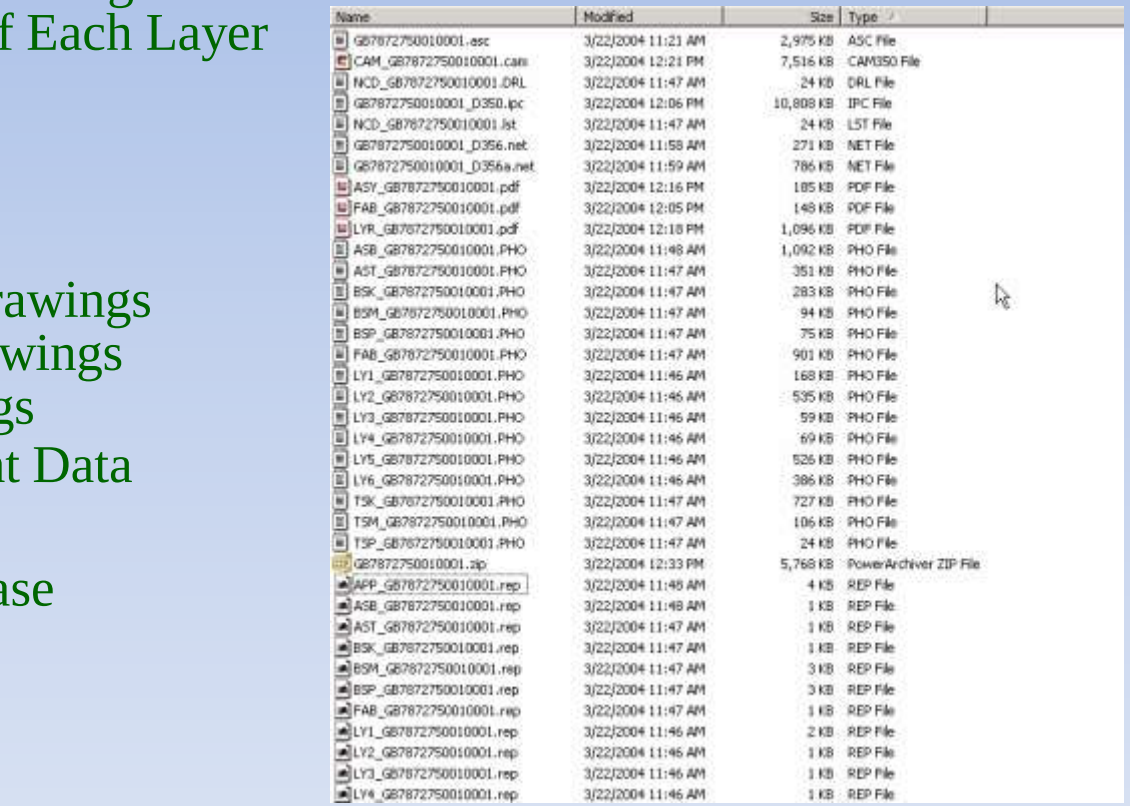
To facilitate electronic assembly, a panel is created around around the pcb.



Finalize Gerber Fabrication Package

All PCB related design data is zipped up for release to the PCB fabricator.

- Fabrication Package
  - Gerber Files of Each Layer
  - Aperture Files
  - Drill Files
  - Netlist files
  - ASCII Files
  - Fabrication Drawings
  - Assembly Drawings
  - Layer Drawings
  - X-Y Placement Data
- Design Release

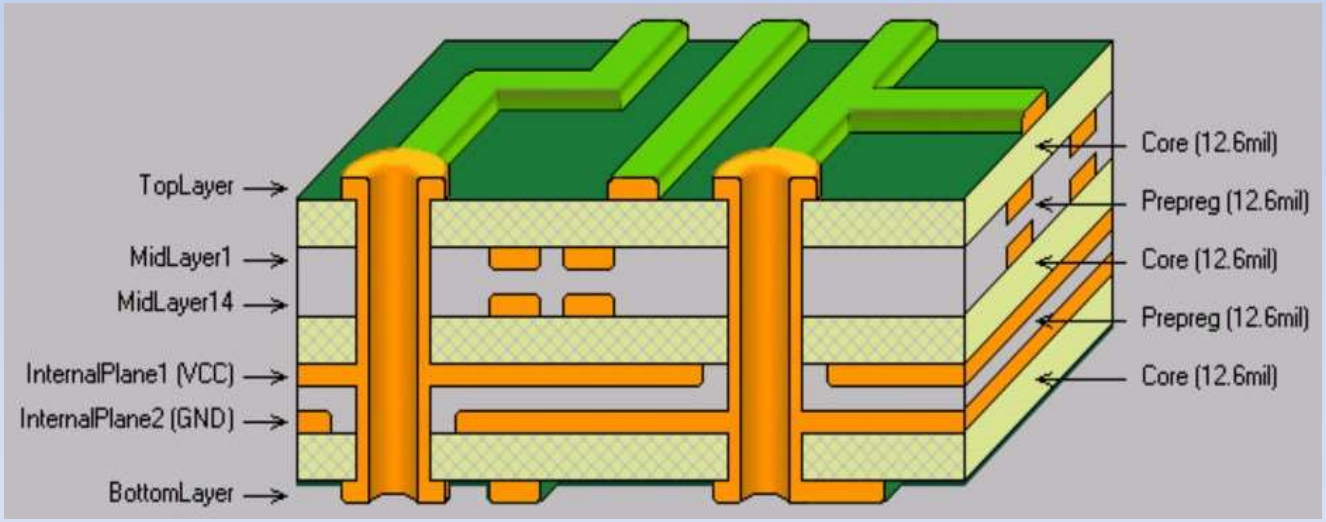


Name	Modified	Size	Type
GB78727500100001.asc	3/22/2004 11:21 AM	2,975 KB	ASC File
CAM_GB78727500100001.cam	3/22/2004 12:21 PM	7,516 KB	CAM350 File
NCD_GB78727500100001.DRL	3/22/2004 11:47 AM	24 KB	DRL File
GB78727500100001_D350.ipc	3/22/2004 12:06 PM	10,808 KB	IPC File
NCD_GB78727500100001.lst	3/22/2004 11:47 AM	24 KB	LST File
GB78727500100001_D356.net	3/22/2004 11:58 AM	271 KB	NET File
GB78727500100001_D356a.net	3/22/2004 11:59 AM	786 KB	NET File
ASY_GB78727500100001.pdf	3/22/2004 12:16 PM	185 KB	PDF File
FAB_GB78727500100001.pdf	3/22/2004 12:05 PM	148 KB	PDF File
LYR_GB78727500100001.pdf	3/22/2004 12:18 PM	1,096 KB	PDF File
ASB_GB78727500100001.PHO	3/22/2004 11:48 AM	1,092 KB	PHO File
AST_GB78727500100001.PHO	3/22/2004 11:47 AM	351 KB	PHO File
BSK_GB78727500100001.PHO	3/22/2004 11:47 AM	283 KB	PHO File
BSM_GB78727500100001.PHO	3/22/2004 11:47 AM	94 KB	PHO File
BSP_GB78727500100001.PHO	3/22/2004 11:47 AM	75 KB	PHO File
FAB_GB78727500100001.PHO	3/22/2004 11:47 AM	901 KB	PHO File
LY1_GB78727500100001.PHO	3/22/2004 11:46 AM	168 KB	PHO File
LY2_GB78727500100001.PHO	3/22/2004 11:46 AM	535 KB	PHO File
LY3_GB78727500100001.PHO	3/22/2004 11:46 AM	59 KB	PHO File
LY4_GB78727500100001.PHO	3/22/2004 11:46 AM	69 KB	PHO File
LY5_GB78727500100001.PHO	3/22/2004 11:46 AM	526 KB	PHO File
LY6_GB78727500100001.PHO	3/22/2004 11:46 AM	386 KB	PHO File
TSK_GB78727500100001.PHO	3/22/2004 11:47 AM	727 KB	PHO File
TSM_GB78727500100001.PHO	3/22/2004 11:47 AM	106 KB	PHO File
TSP_GB78727500100001.PHO	3/22/2004 11:47 AM	24 KB	PHO File
GB78727500100001.zip	3/22/2004 12:33 PM	5,768 KB	PowerArchiver ZIP File
APP_GB78727500100001.rep	3/22/2004 11:48 AM	4 KB	REP File
ASB_GB78727500100001.rep	3/22/2004 11:48 AM	1 KB	REP File
AST_GB78727500100001.rep	3/22/2004 11:47 AM	1 KB	REP File
BSK_GB78727500100001.rep	3/22/2004 11:47 AM	1 KB	REP File
BSM_GB78727500100001.rep	3/22/2004 11:47 AM	3 KB	REP File
BSP_GB78727500100001.rep	3/22/2004 11:47 AM	3 KB	REP File
FAB_GB78727500100001.rep	3/22/2004 11:47 AM	1 KB	REP File
LY1_GB78727500100001.rep	3/22/2004 11:46 AM	2 KB	REP File
LY2_GB78727500100001.rep	3/22/2004 11:46 AM	1 KB	REP File
LY3_GB78727500100001.rep	3/22/2004 11:46 AM	1 KB	REP File
LY4_GB78727500100001.rep	3/22/2004 11:46 AM	1 KB	REP File

PCB Fabrication

PCB Basics

- Basic PCBs comprise a rigid sheet of epoxy-impregnated fiberglass material within copper sheets affixed to one or both sides. This is known as copper clad. In multilayer boards (those with more than two copper layers), a piece of material called prepreg is placed between core layers.



PCB Fabrication

PCB Basics (continued)

- The outer copper surface of the PCB must be processed to form circuit paths, or traces, that make the connections between components. Analogous to wires, the traces are formed using a photolithographic process. In that process, the copper layers are treated with chemical etching that removes unneeded portions of the copper, leaving only the traces and pads required for component soldering.

- Pads can be fabricated in many shapes and formats. Components are typically attached to these pads as surface mount, through hole, or both. After photolithography is completed, the board is drilled and through holes are plated.

PCB Fabrication

Process

For multi-layer designs, the first step is to print etch the inner layers. Each inner circuit is transferred to the copper panel using photographic dry film. The film is hot-roll laminated onto the copper panel. The film tooling is exposed onto the panel typically using a 5-kilo Watt light source. The panels are put through a series of vertical conveyors containing various wet processing chemicals. First, the exposed film on the panels is developed, then the exposed copper (no film on it) is etched away and finally the remaining film is stripped off resulting in bare copper circuits on laminate. This process usually takes about three hours.

The inner layers are then pinned in a stack with thin sheets of epoxy glass pre-preg which separates the copper layers. The outer layers are made with a foil of copper. The stack is pinned between two heavy metal plates creating a "book." This book is put in a hydraulic/heated press for about two hours at 350 degrees F. The hydraulic pressure is approximately three tons.

PCB Fabrication

Process (continued)

Once pressed, these panels look just like double sided laminate and are ready for drilling. For double-sided panels, drilling is the first process. The panels are pinned to the table of a CNC drill. The drill program is loaded, and the proper drill bit sizes are loaded into the auto-tool-change holders. A typical load size is 15 panels up. The panels are then deburred after drilling. This process usually lasts anywhere from 30 minutes to two hours.

Electroless copper is next. In order to put a thin (0.000025") coat of copper inside the drilled holes, there is a series of chemicals required to condition, clean, and activate the surface inside the holes. The panels sit in a blue liquid of suspended copper for about 45 minutes; the entire process takes about two hours.

Primary image (i.e., the top & bottom layers) is applied using dry film plating resist, as before with the inner layers. It is developed, and then it goes into a copper plating procedure. The panels are cleaned and activated chemically, then connected to a rack inside a large volume of copper solution.

PCB Fabrication

Process (continued)

At 25 amps/square foot of copper, the panels are electro-plated for about one hour to achieve one ounce of copper in the holes and on the surface. Next, tin is plated on top of the copper. (During the entire time, the dry film (plating resist) is on the panels to prevent plating where there are no circuits.)

After plating, the dry film plating resist is stripped off the panel leaving exposed copper. This copper is chemically etched off the panel leaving only the tin over copper circuitry. Next, the tin is stripped from the panel leaving bare copper circuits.

Solder Mask is applied directly over the bare copper. Liquid Photo Imagable (LPI) Solder Mask is flooded onto the panel using a screen. It is then tack dried in a convection oven. The panel is aligned to the Solder Mask tooling film using registration pins and then exposed in a 5 kW light source for about 20 seconds. The panel is then developed to remove LPI Solder Mask from the pads and holes. Finally, the panel is baked to cure the remaining mask to its permanent state. The total LPI time is about two hours.

PCB Fabrication

Process (continued)

Legend ink (silkscreen) is screened onto the panel using a screen stencil, which is photographically made from the Legend film work. The panel is cured in a convection oven to complete the screening process in about an hour.

Next, the panel is put through a Hot Air Solder Leveler (HASL) in order to put solder on the pads and in the holes. It consists of a flux tank, a solder tank at about 360 degrees F, and air knives to blow out the holes.

The CNC routing is the final step to the pcb fabrication process. The panels are pinned to a backup material. The CNC program is loaded into memory, and a router bit is placed in the tool changer. Normally, an 0.093" size bit is used. The parts are routed out individually. Gold fingers, if present, are then beveled.

END